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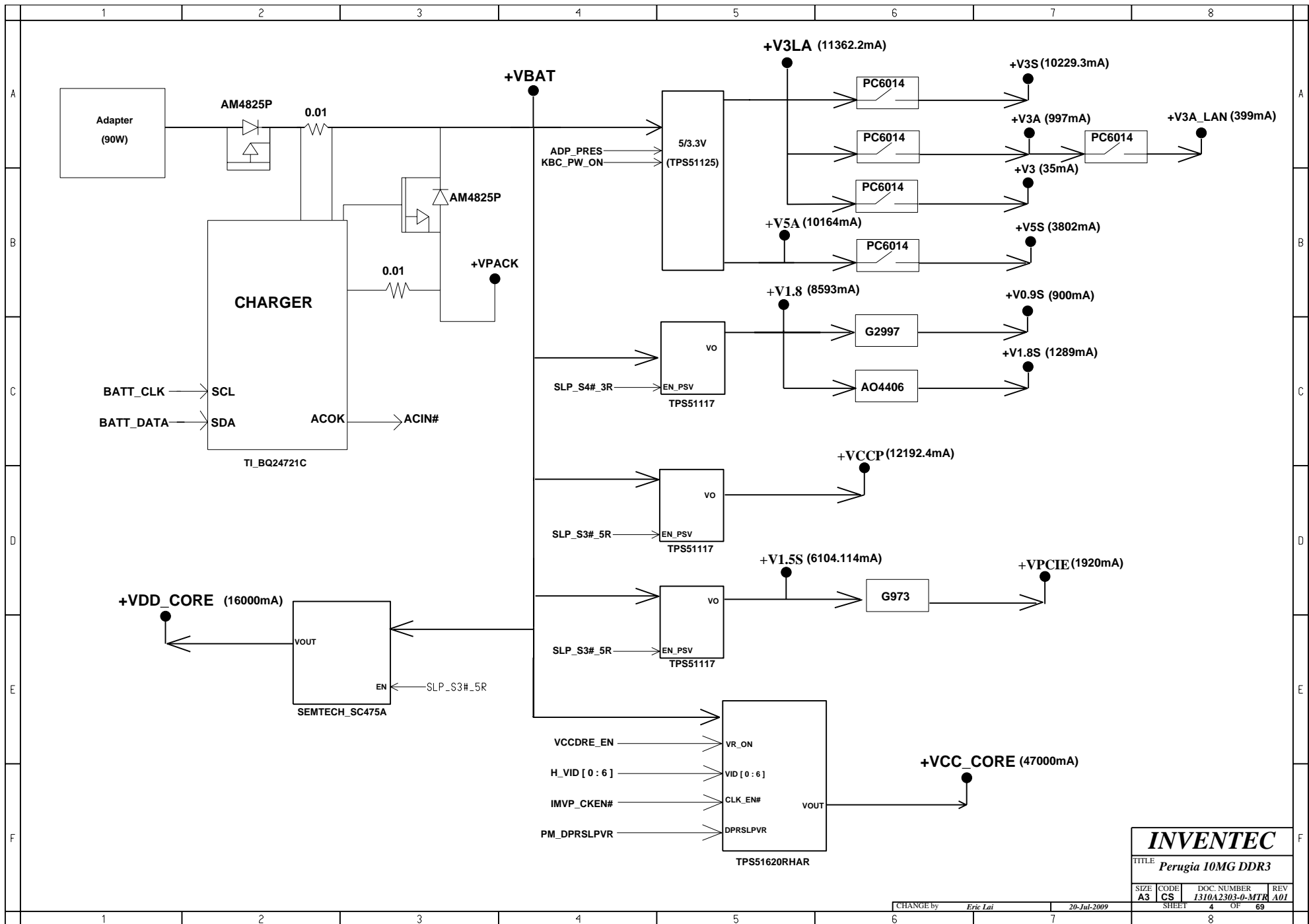
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INVENTEC

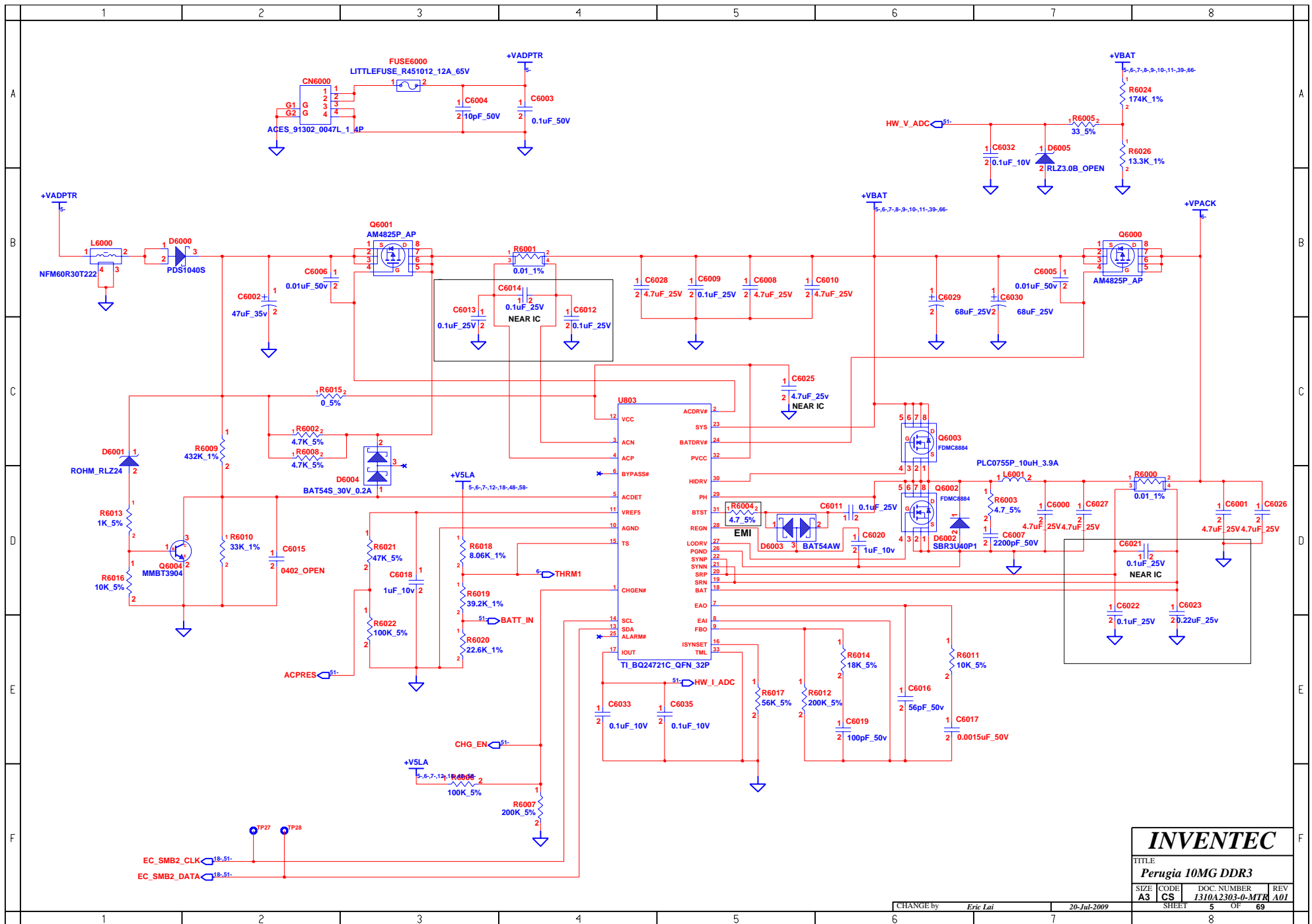
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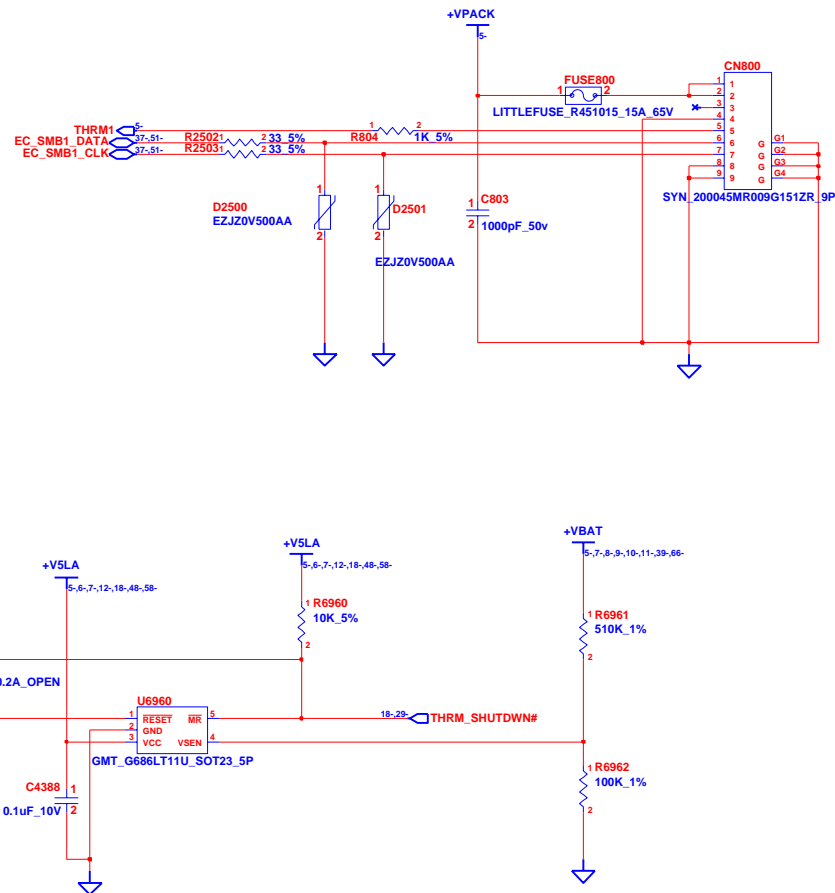
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CHANGE by **Eric Lai** 20-Jul-2009



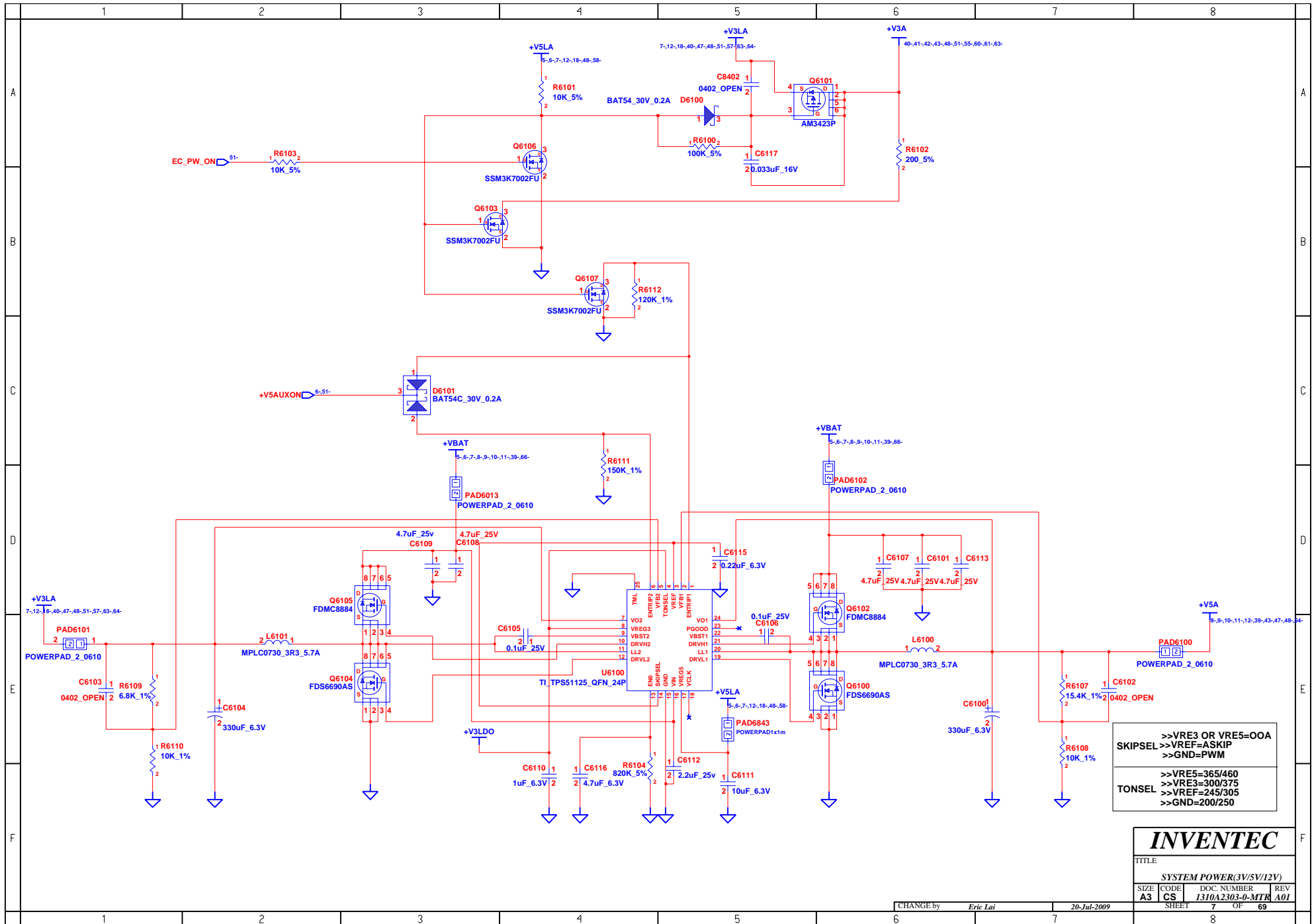
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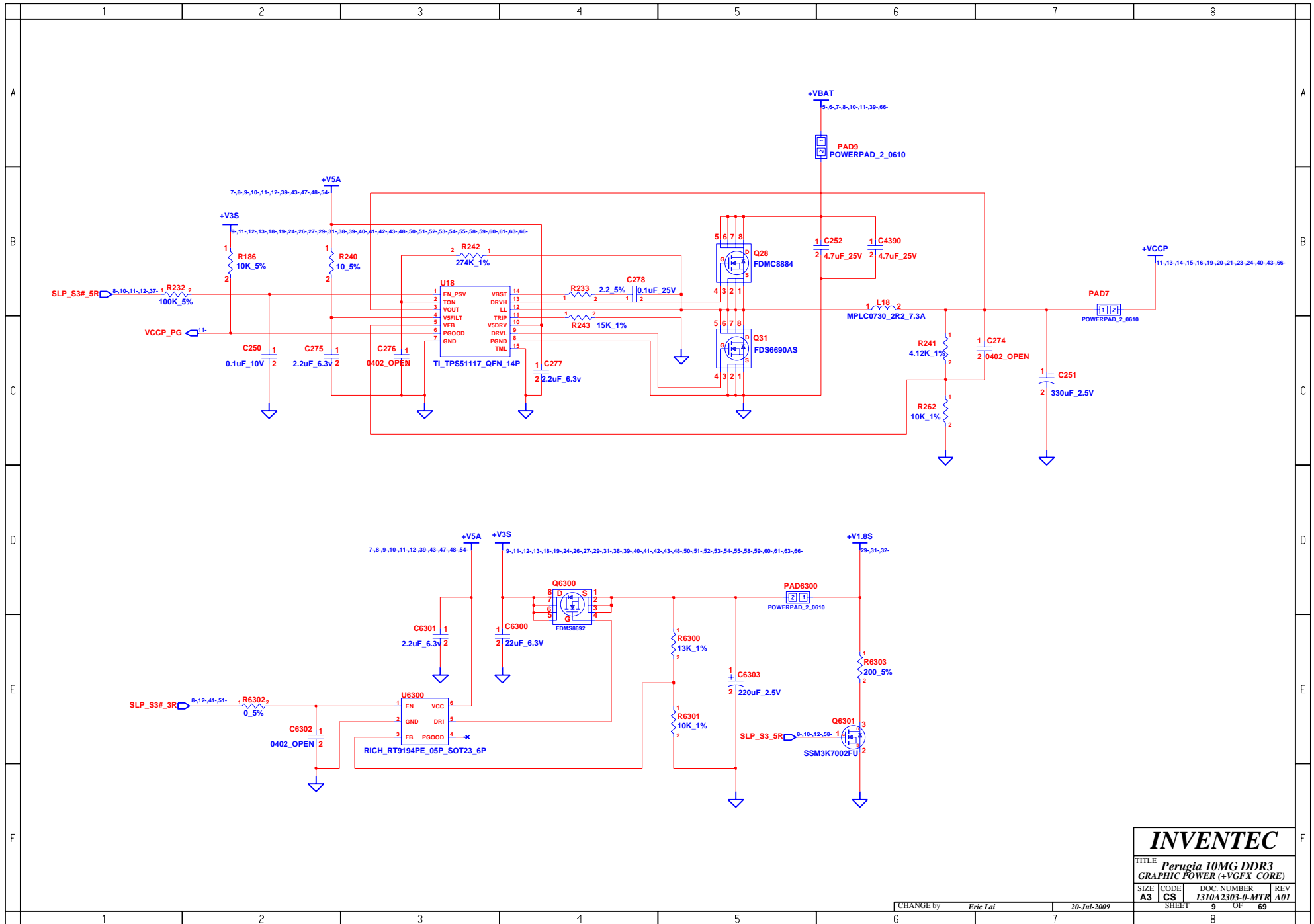


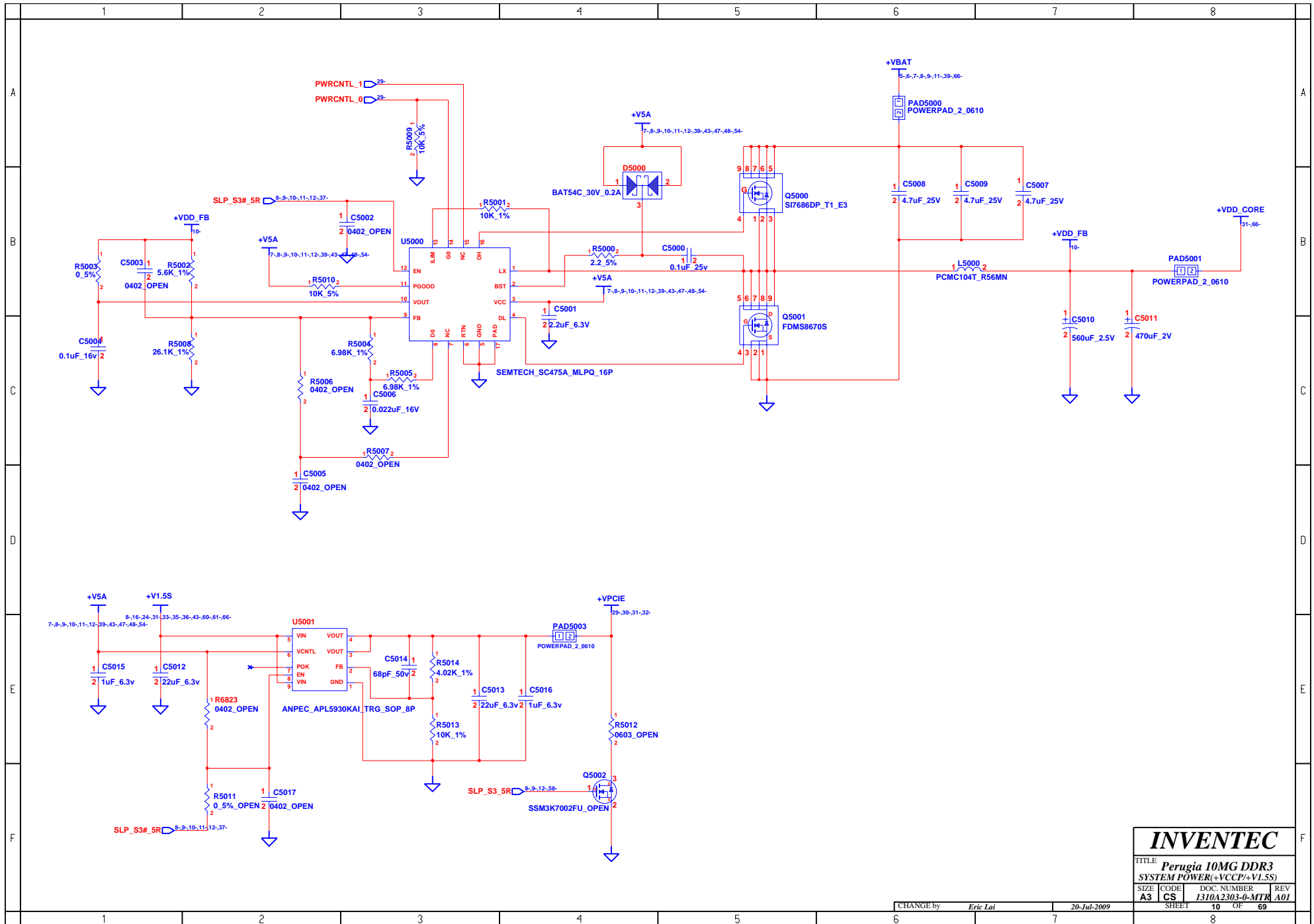


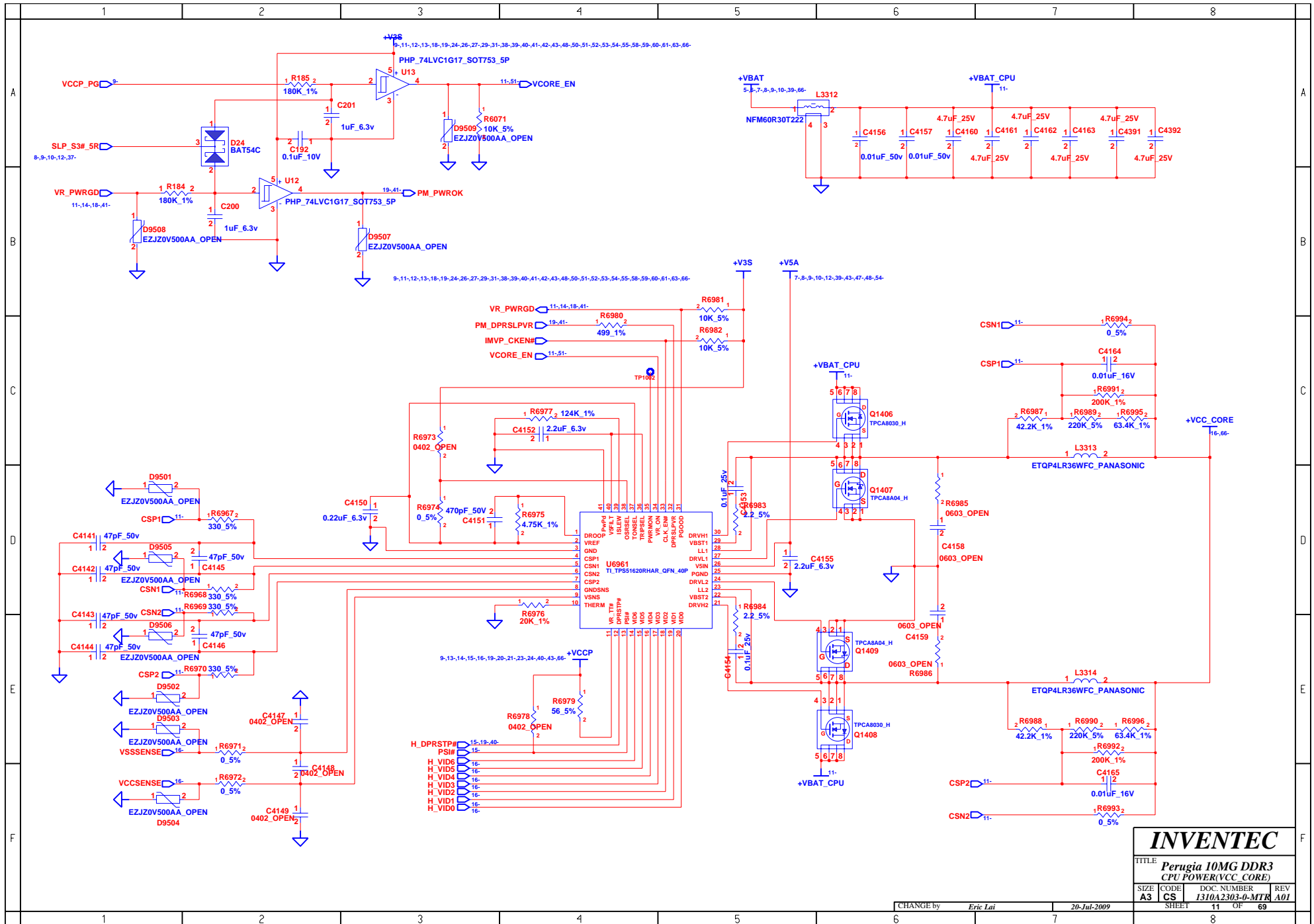
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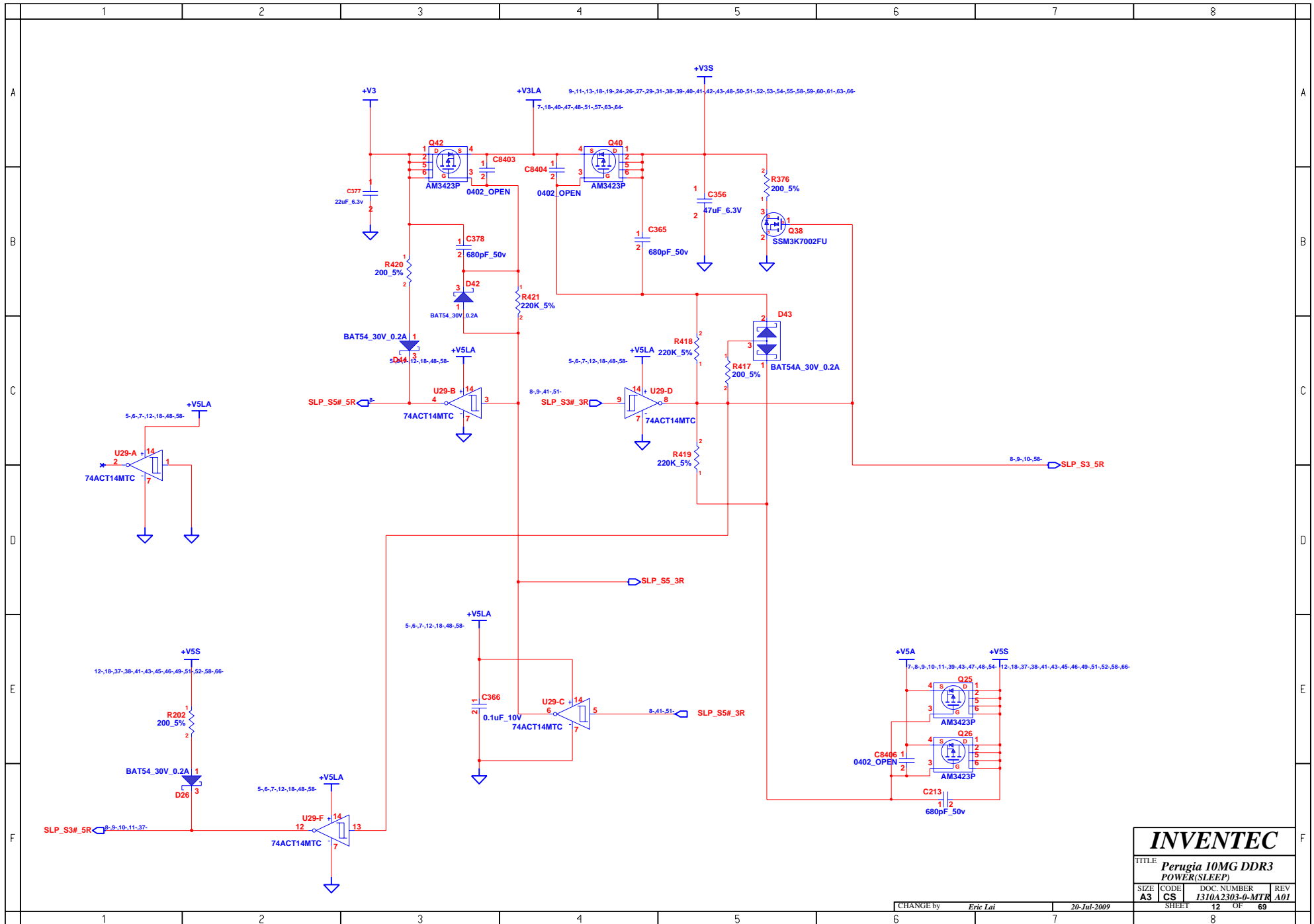




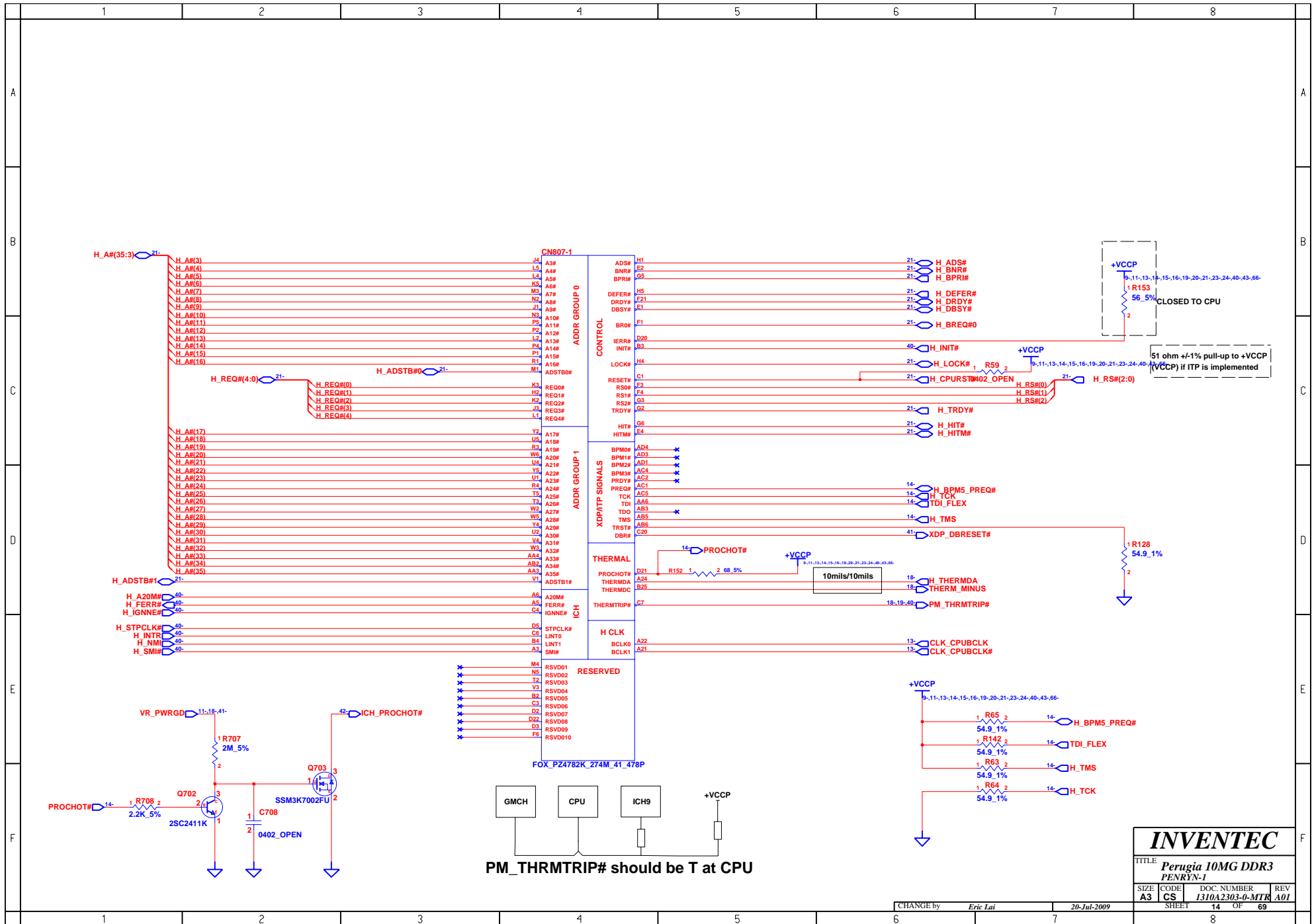


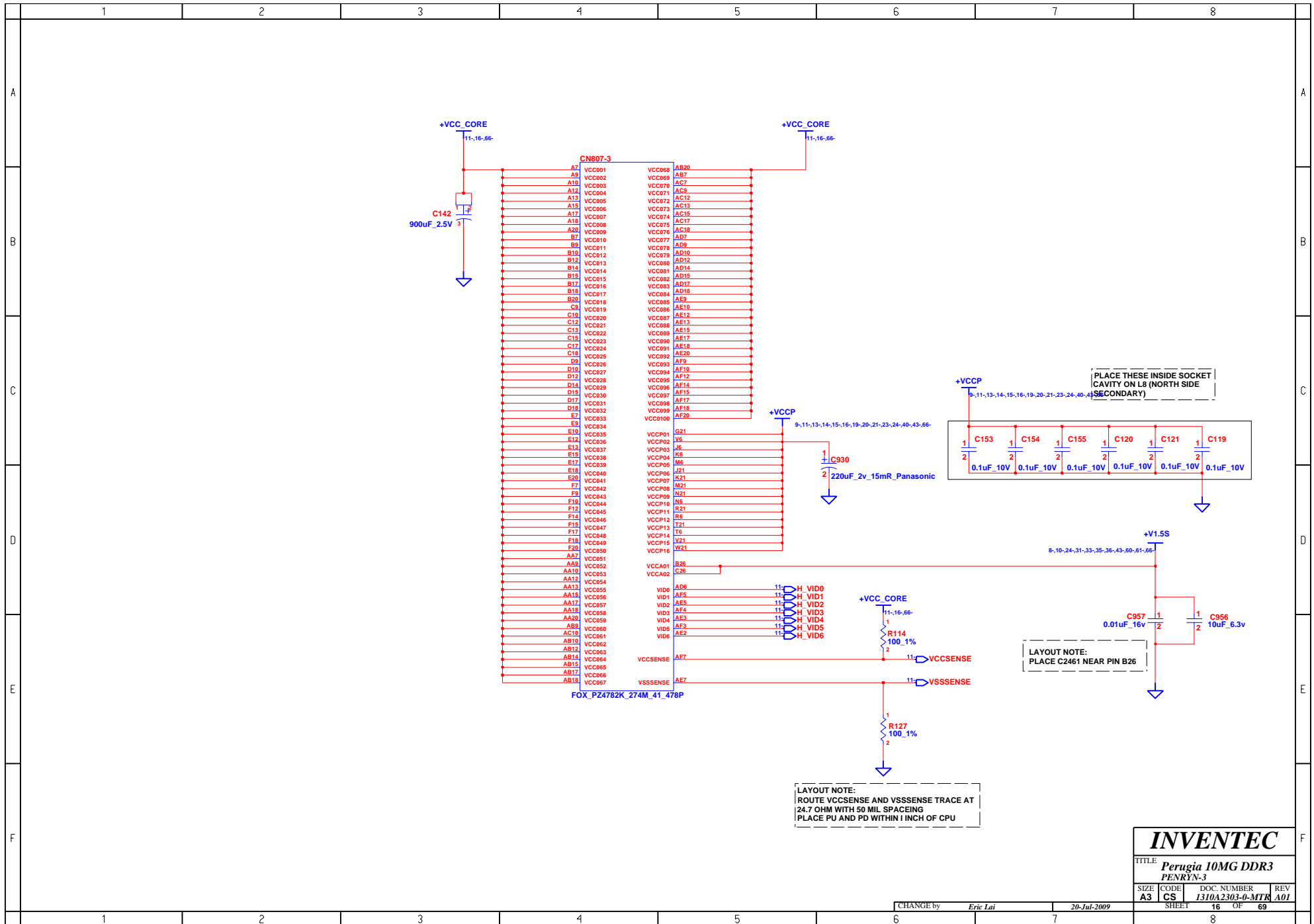
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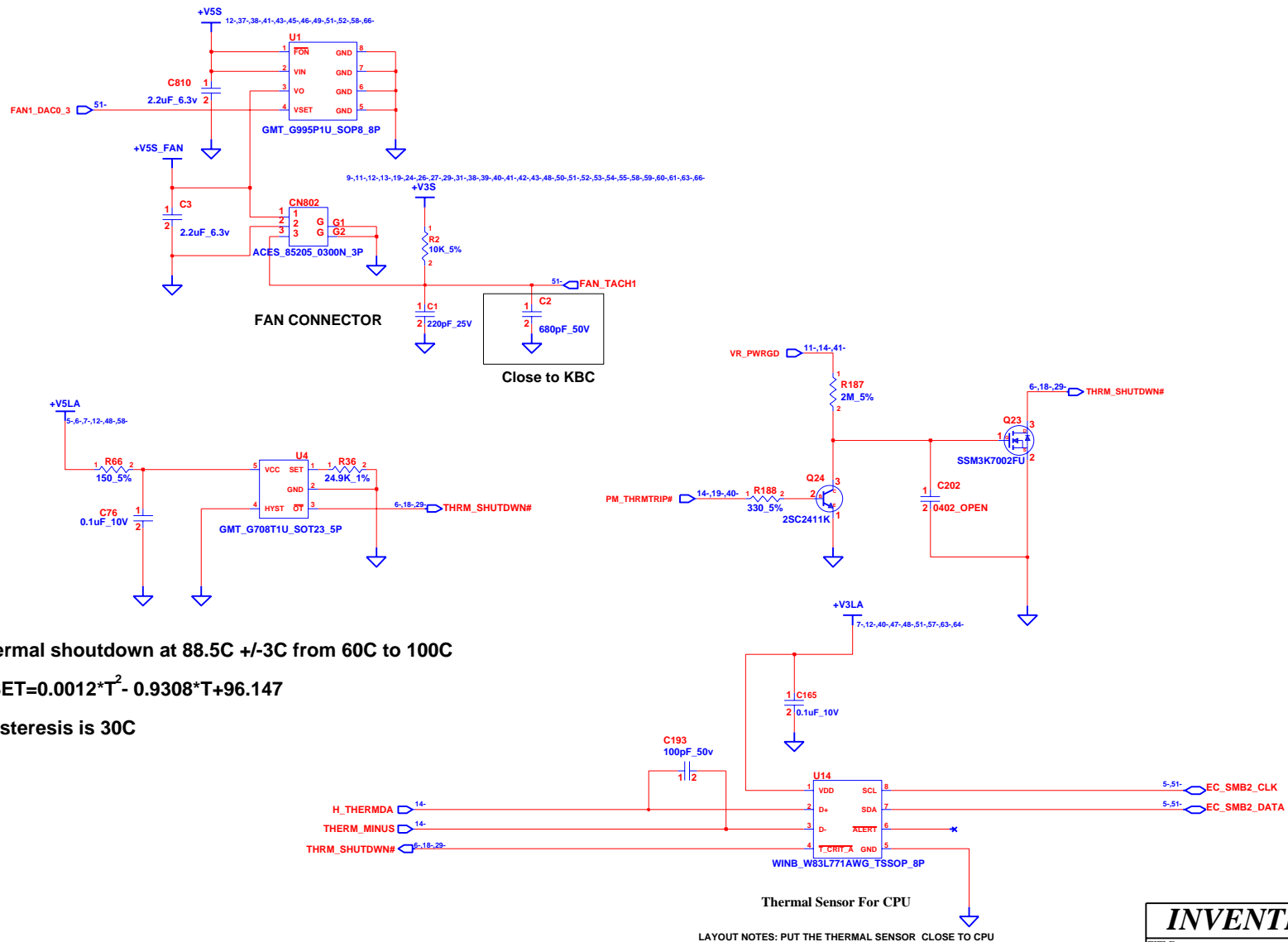
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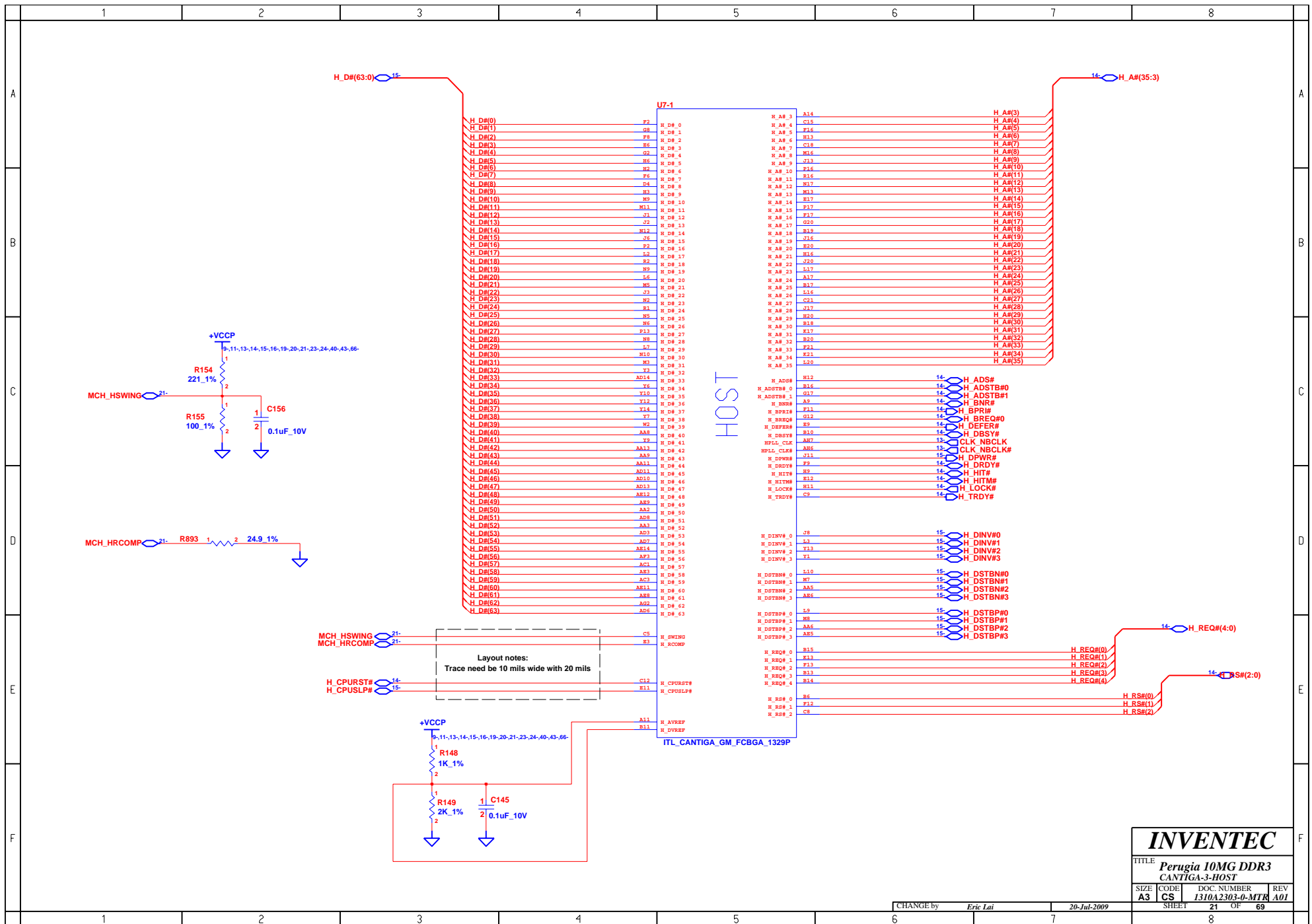
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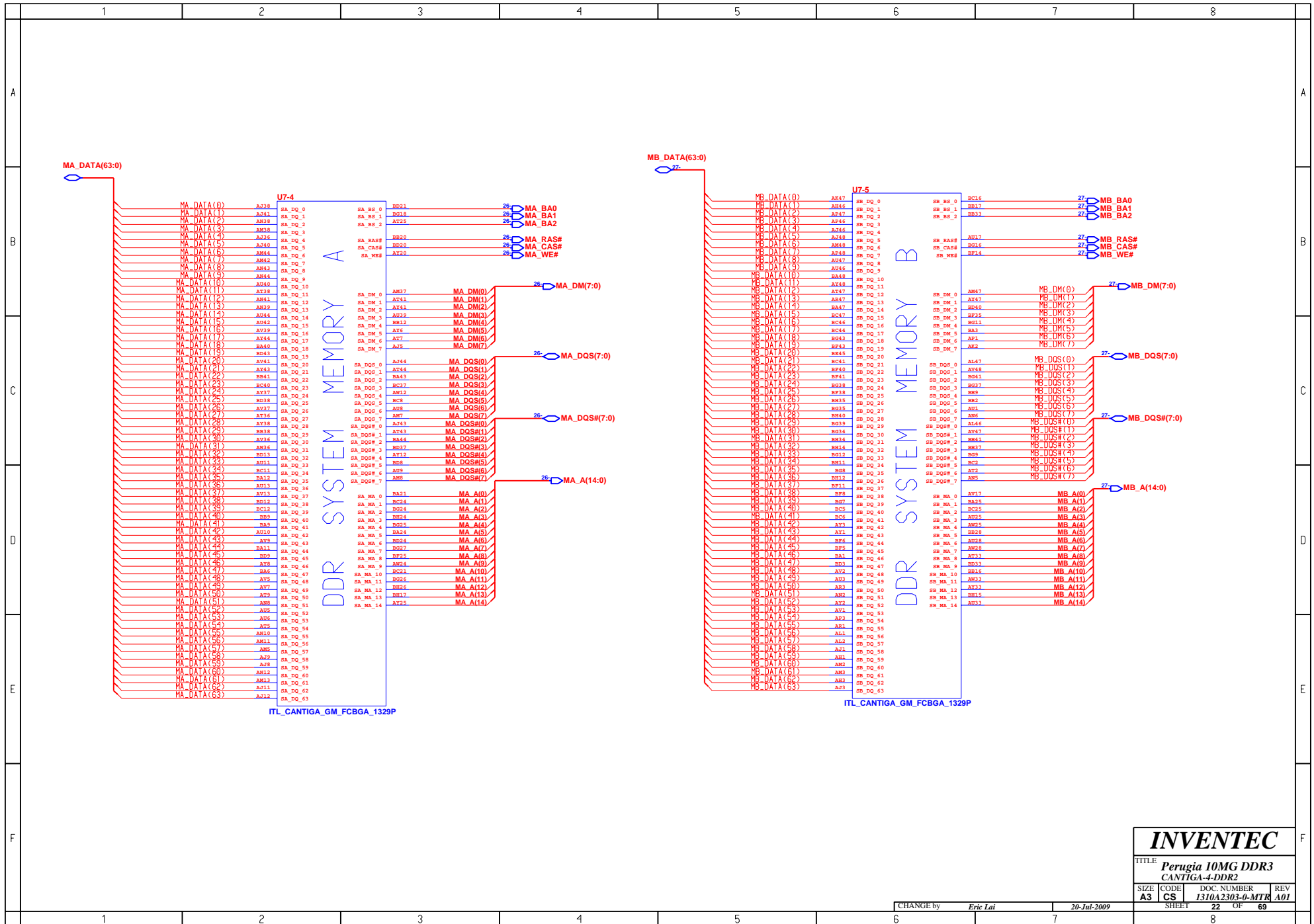


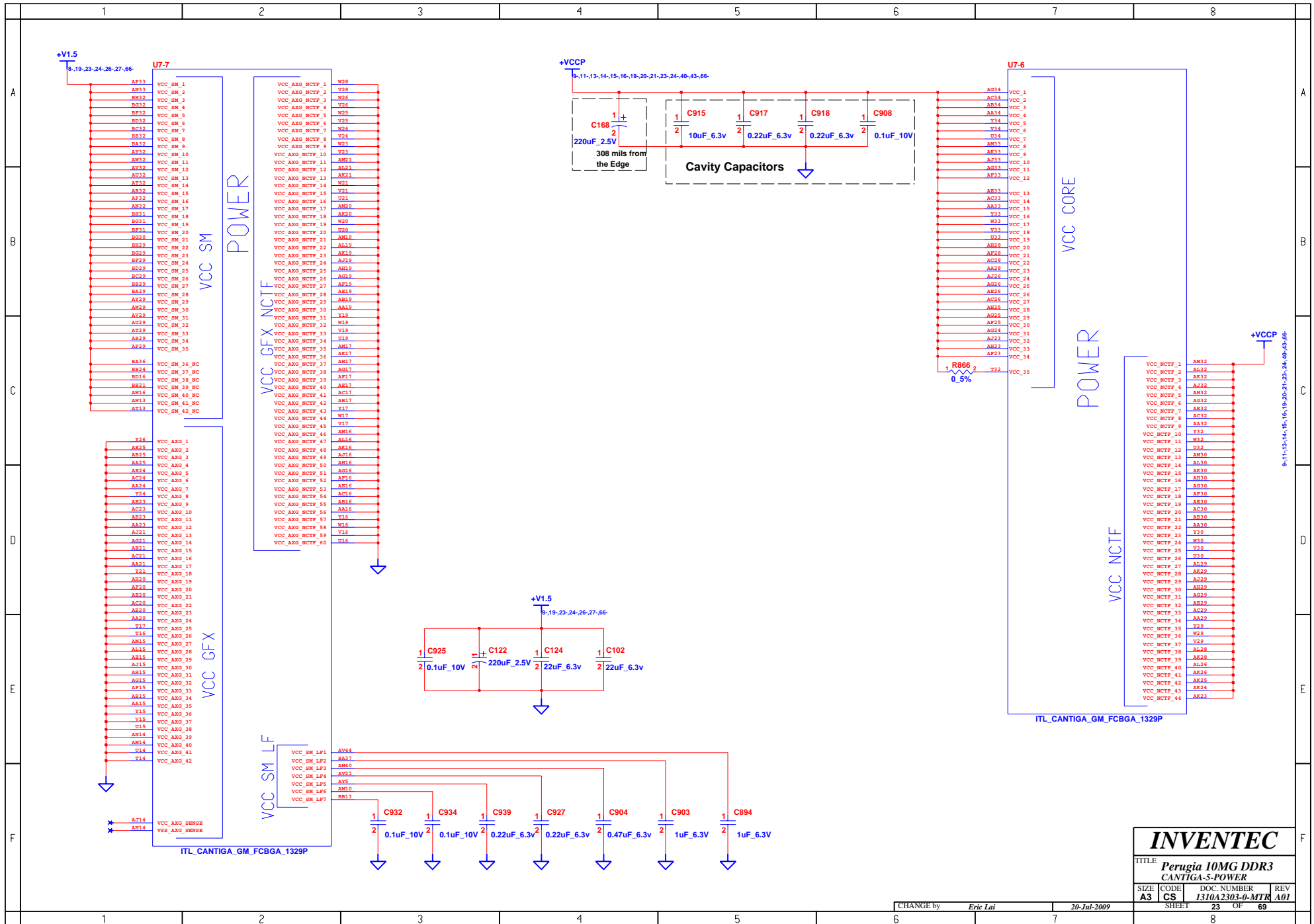


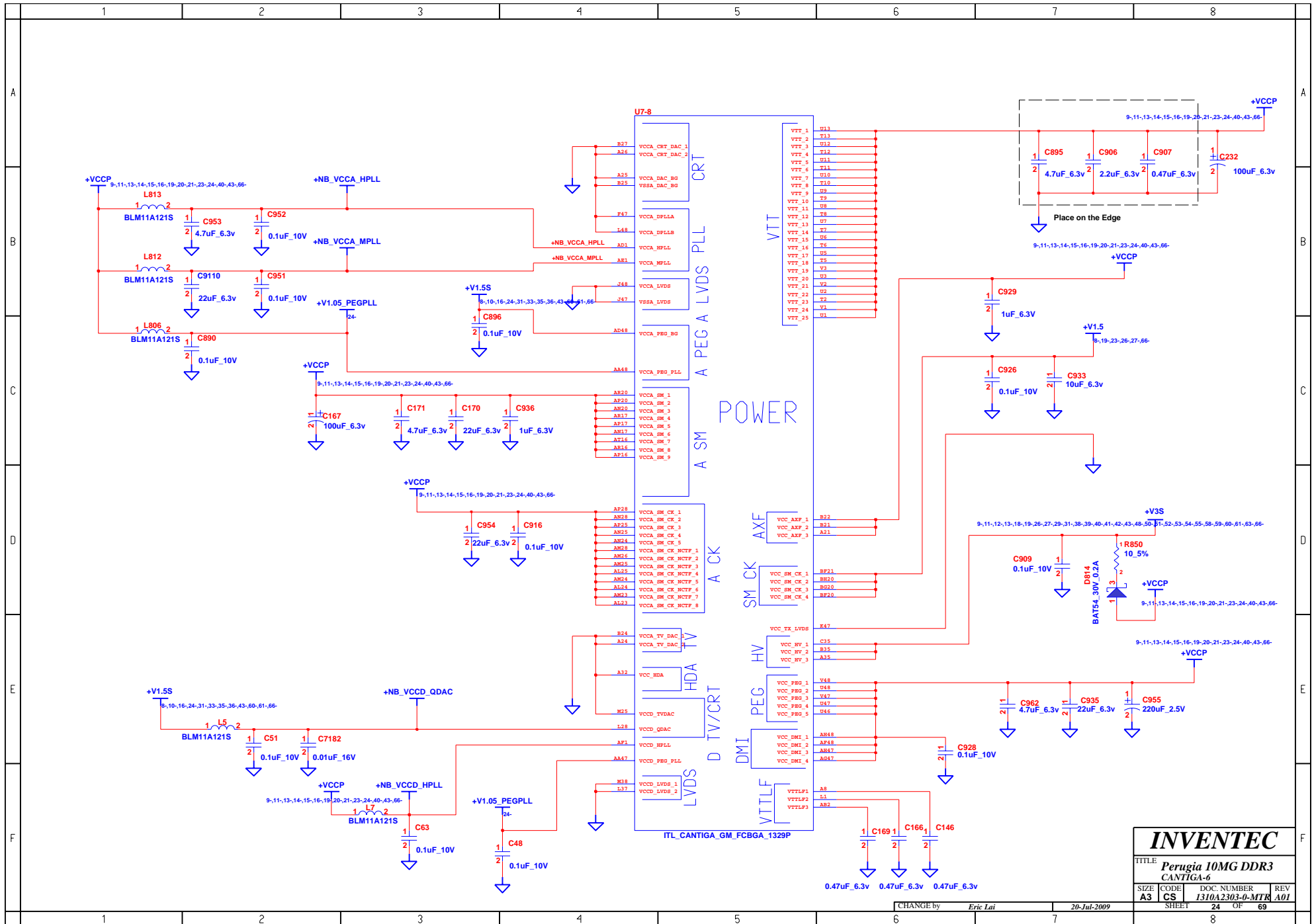


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CHANGE by Eric Lai		20-Jul-2009	
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VSS

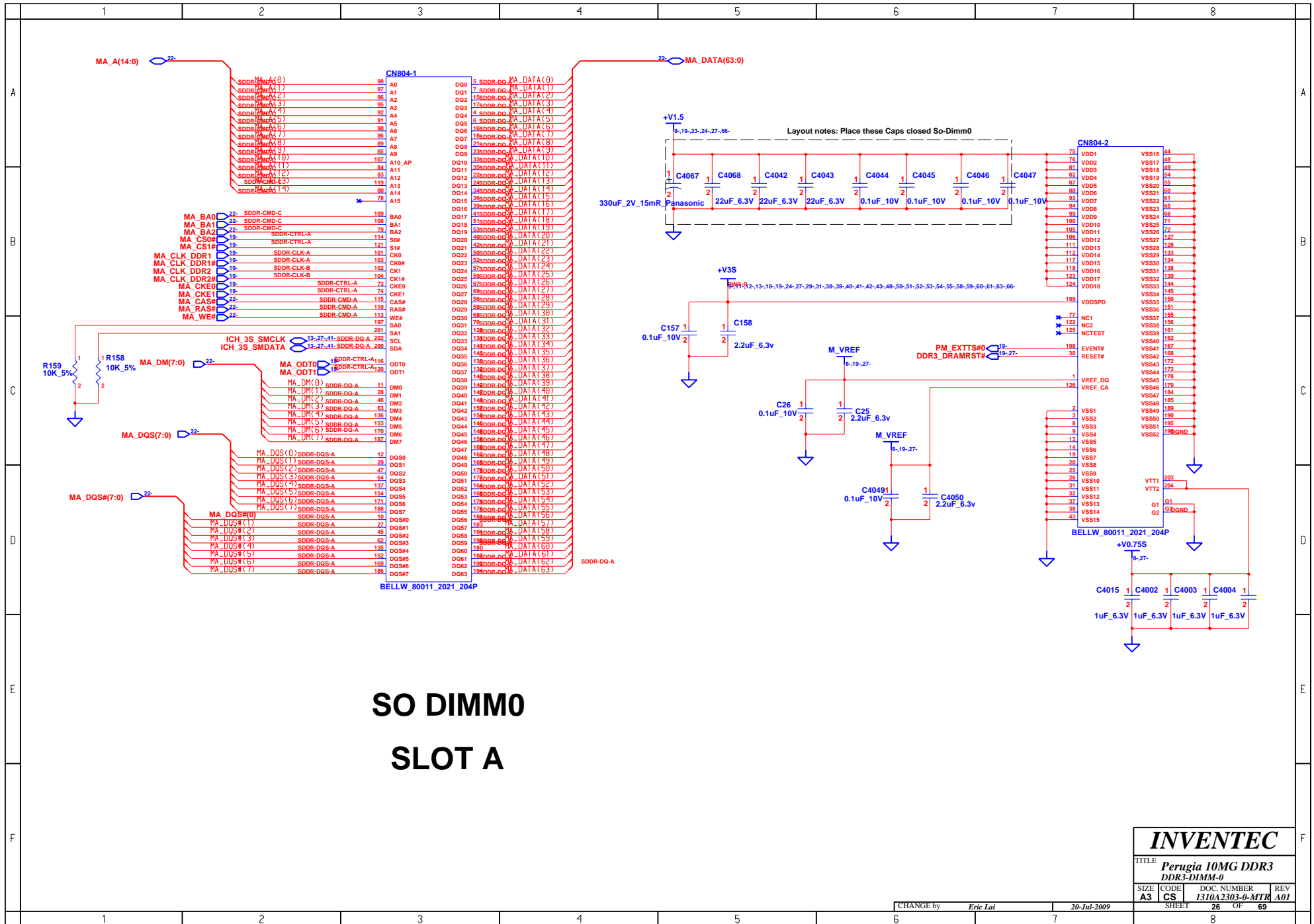
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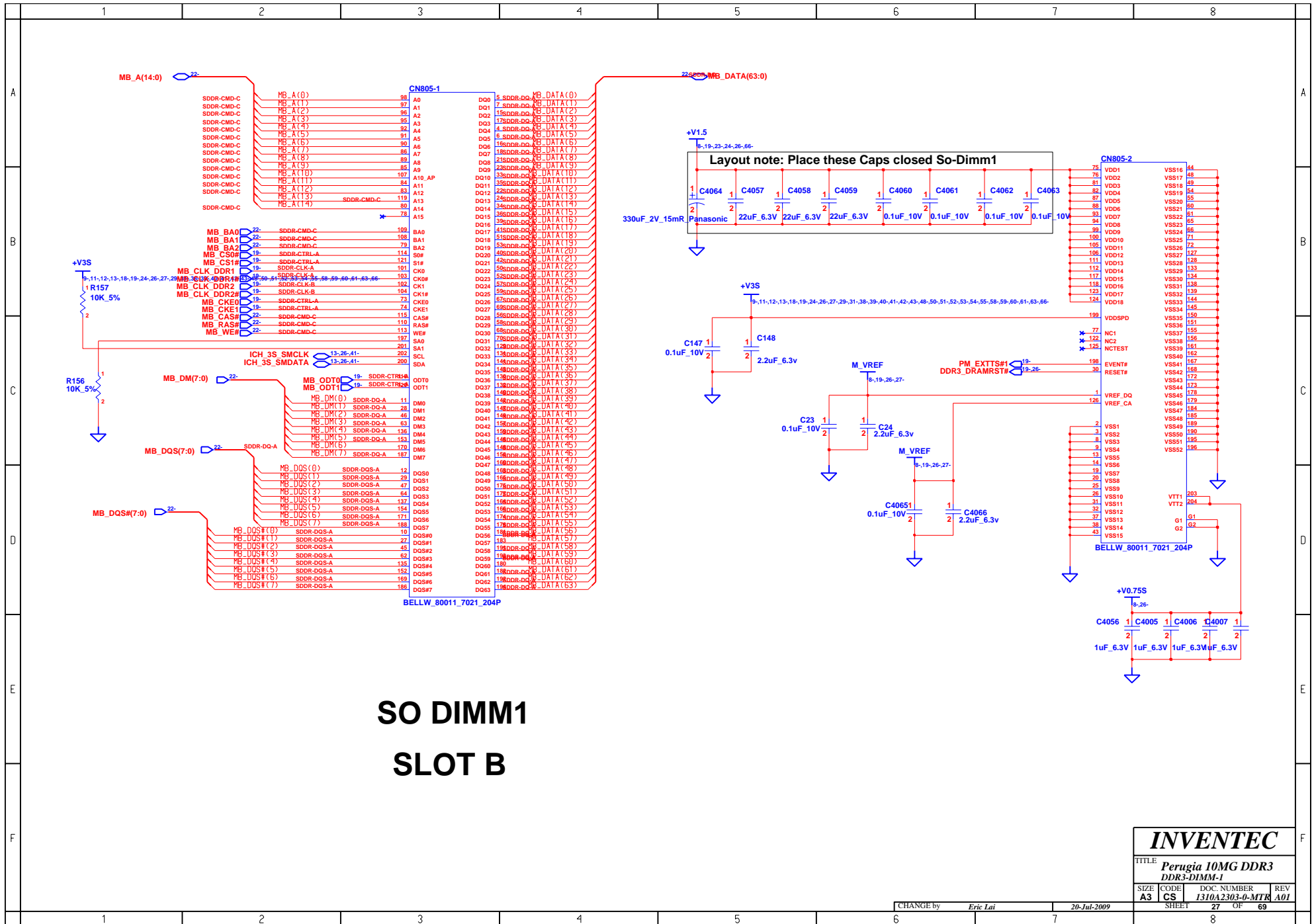
VSS

VSS

VSS

VSS



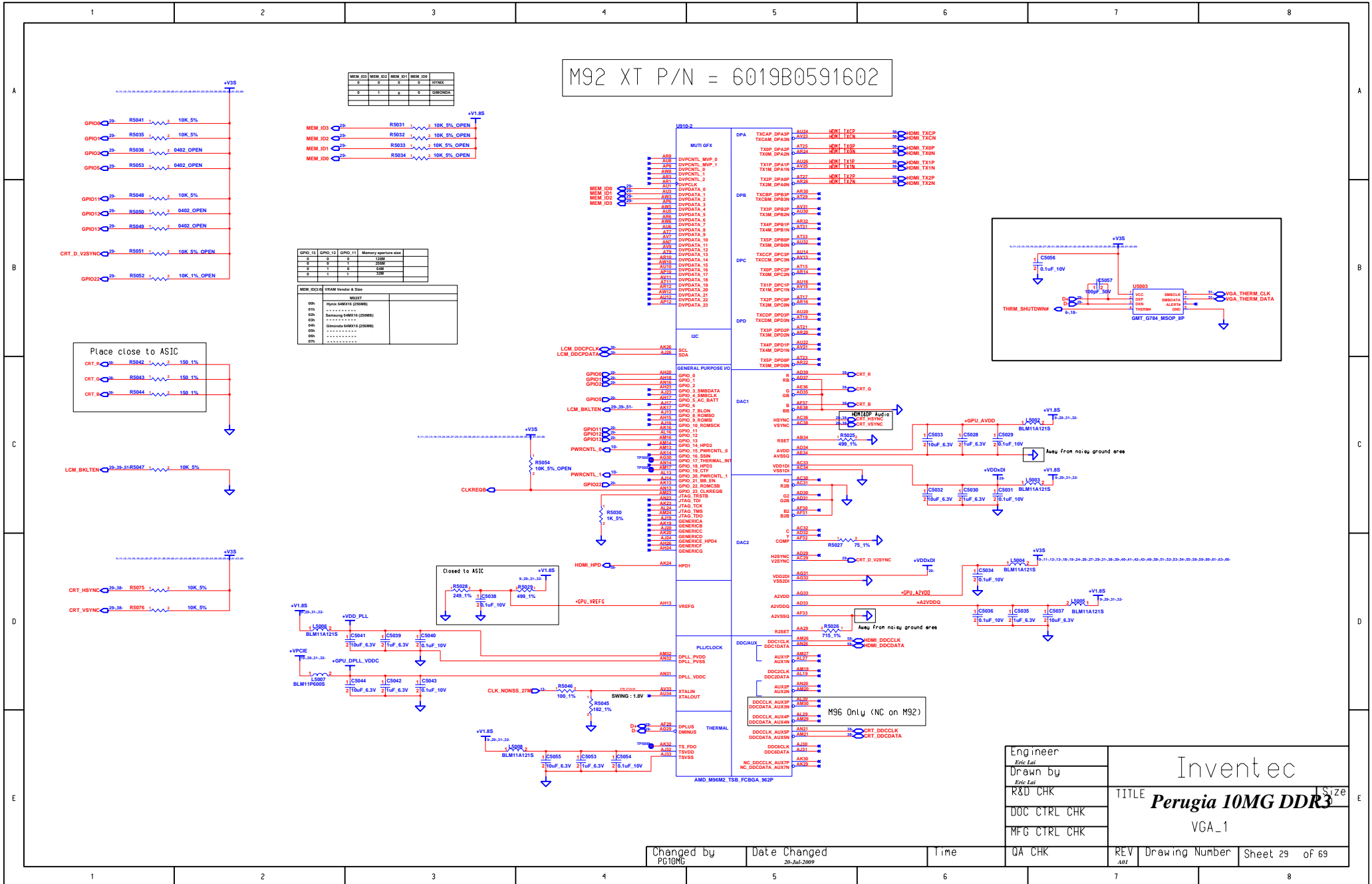


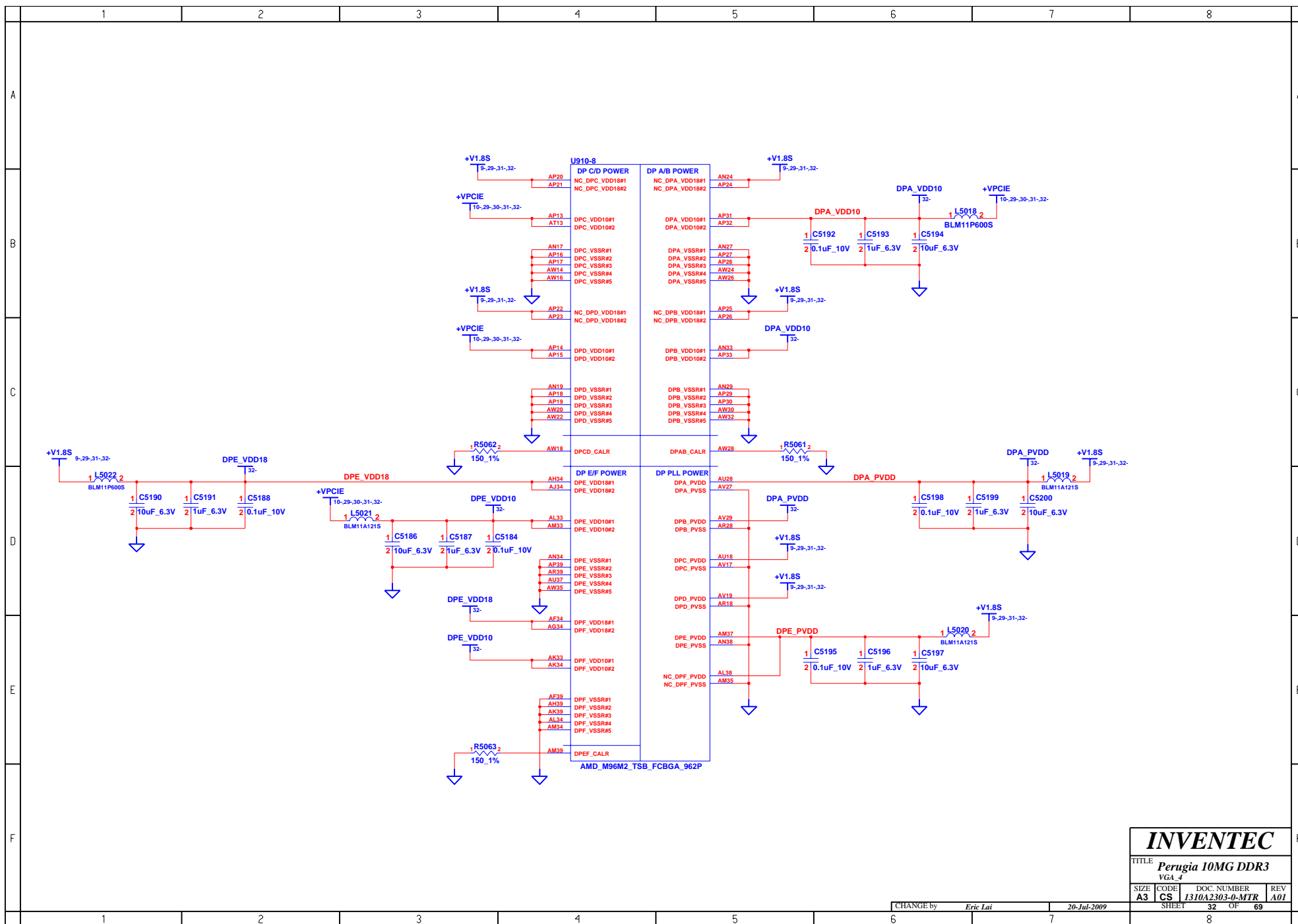
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B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

INVENTEC			
TITLE Perugia 10MG DDR3 DDR2-DAMPING			
SIZE A3	CODE CS	DOC. NUMBER I310A2303-0-MTR	REV A01
SHEET		28	OF 69

CHANGE by **Erie Lal** 27-Sep-2003

M92 XT P/N = 6019B0591602





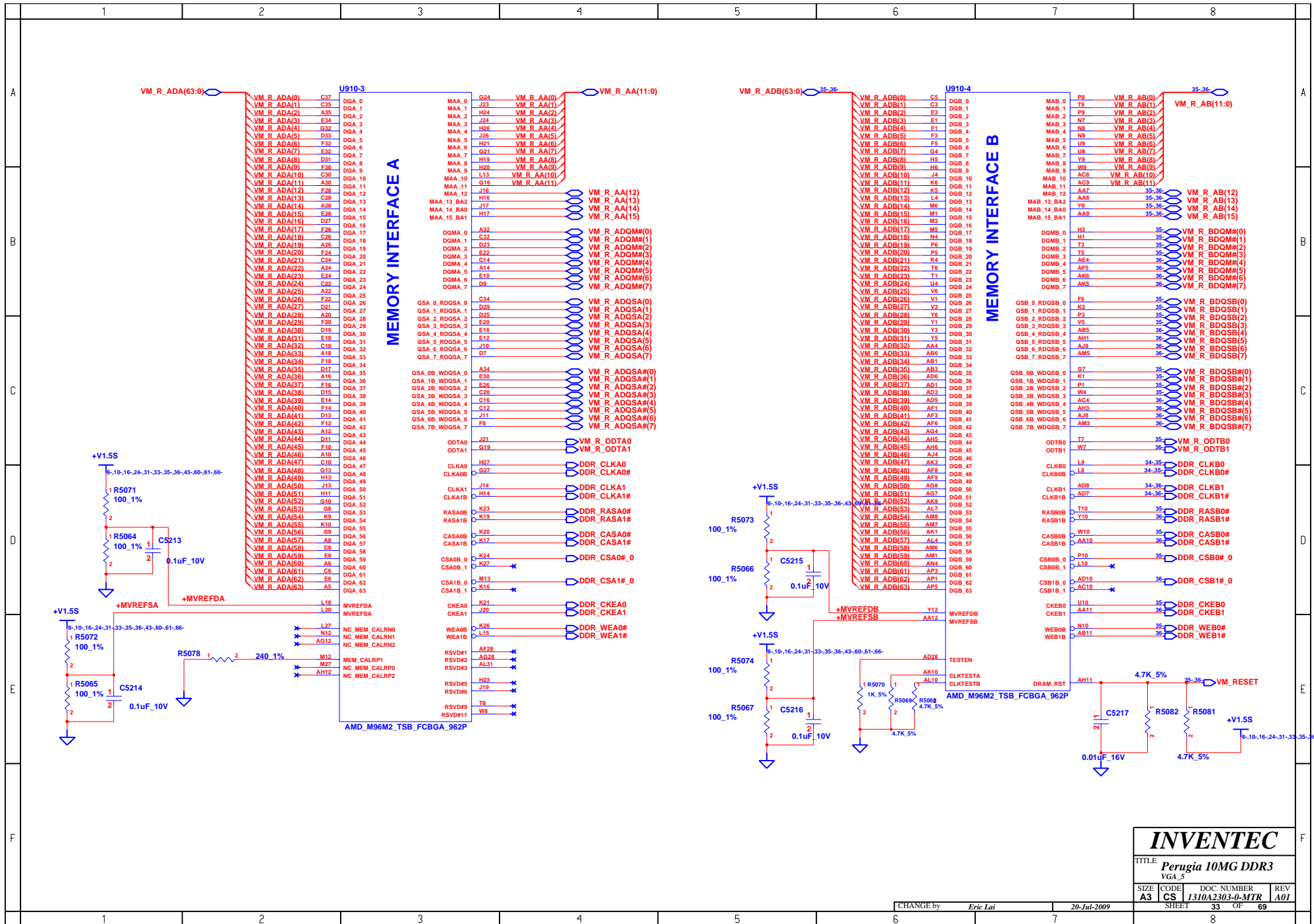
INVENTEC

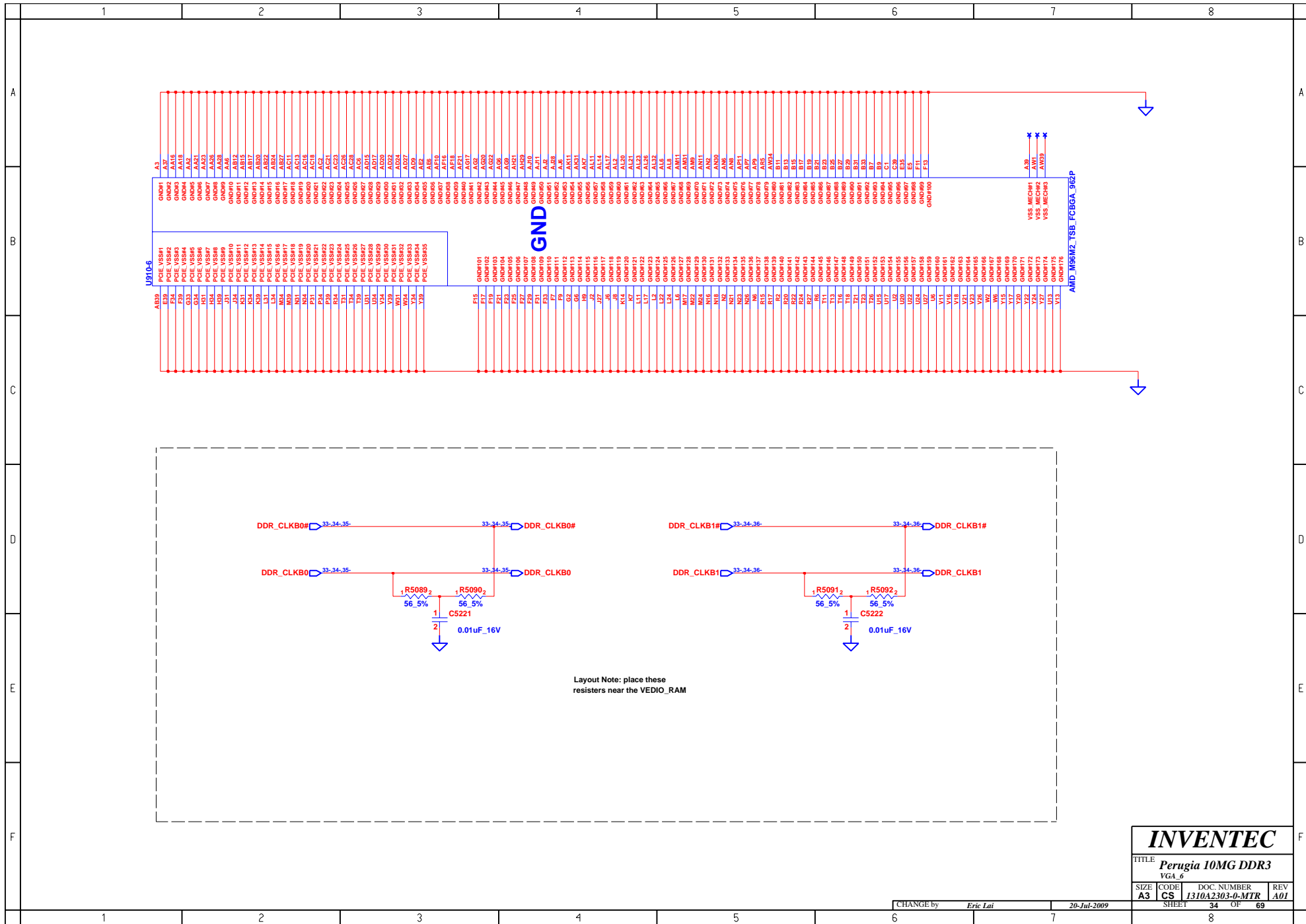
TITLE
VGA_4
Perugia 10MG DDR3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A2303-0-MTR	A01

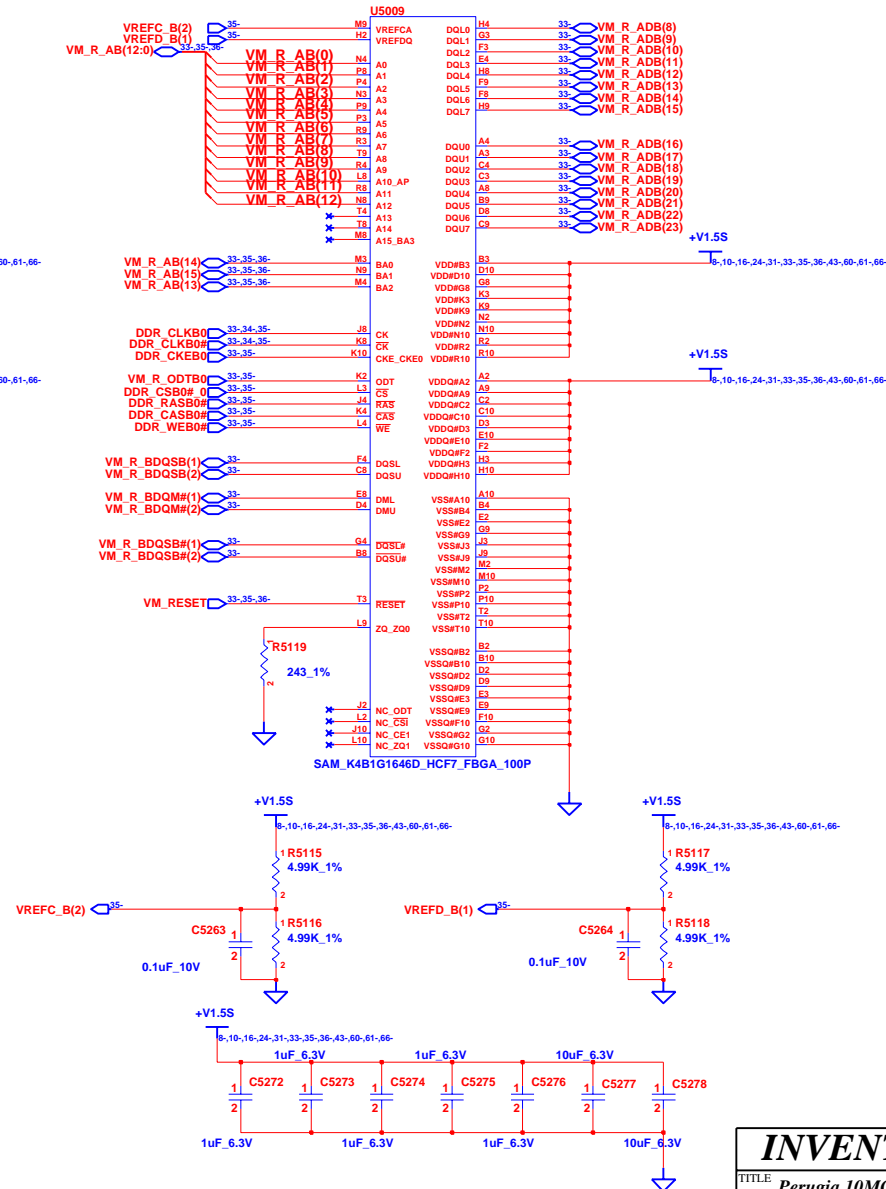
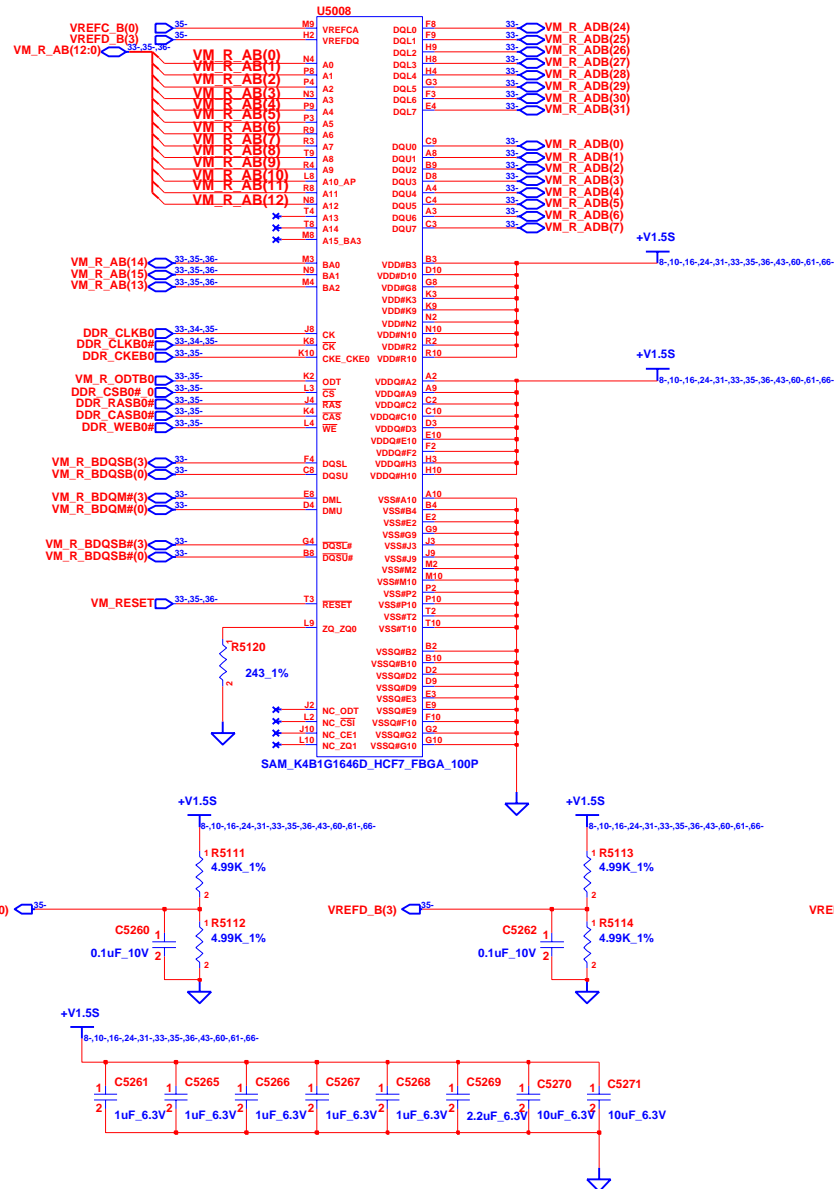
CHANGE by Eric Lai 20-Jul-2009

SHEET 32 OF 69





M92 Use channel B



INVENTEC

TITLE
Perugia 10MG DDR3

SIZE CODE DOC. NUMBER REV
A3 CS 1310A2303-0-MTR A01

CHANGE by Eric Lai 20-Jul-2009

SHEET 35 OF 69

M92 Use channel B

The diagram illustrates the PCB layout for two channels, U5010 and U5011, which are M92 memory modules. The layout includes the following components and connections:

- U5010 and U5011:** The main memory modules, each with 33 pins. They are connected to the system bus via channel B.
- Power and Ground:** The modules are powered by +V1.5S. Ground connections are provided for pins 8, 10, 16, 24, 31, 33, 35, 36, 43, 60, 61, and 66.
- Resistors:** Various resistors are used for termination and signal conditioning, including R5120, R5121, R5122, R5123, R5124, R5125, R5126, R5127, R5128, R5129, R5130, and R5131.
- Capacitors:** Capacitors are used for decoupling and timing, including C5279, C5280, C5281, C5282, C5283, C5284, C5285, C5286, C5287, C5288, C5289, C5290, C5291, C5292, C5293, C5294, C5295, C5296, and C5297.
- Signal Connections:** The modules are connected to the system bus via pins 33, 35, 36, 43, 60, 61, and 66.

Channel U5010:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5011:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5012:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5013:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5014:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5015:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5016:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5017:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5018:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5019:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5020:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5021:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5022:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5023:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5024:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5025:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5026:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5027:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5028:

- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

Channel U5029:

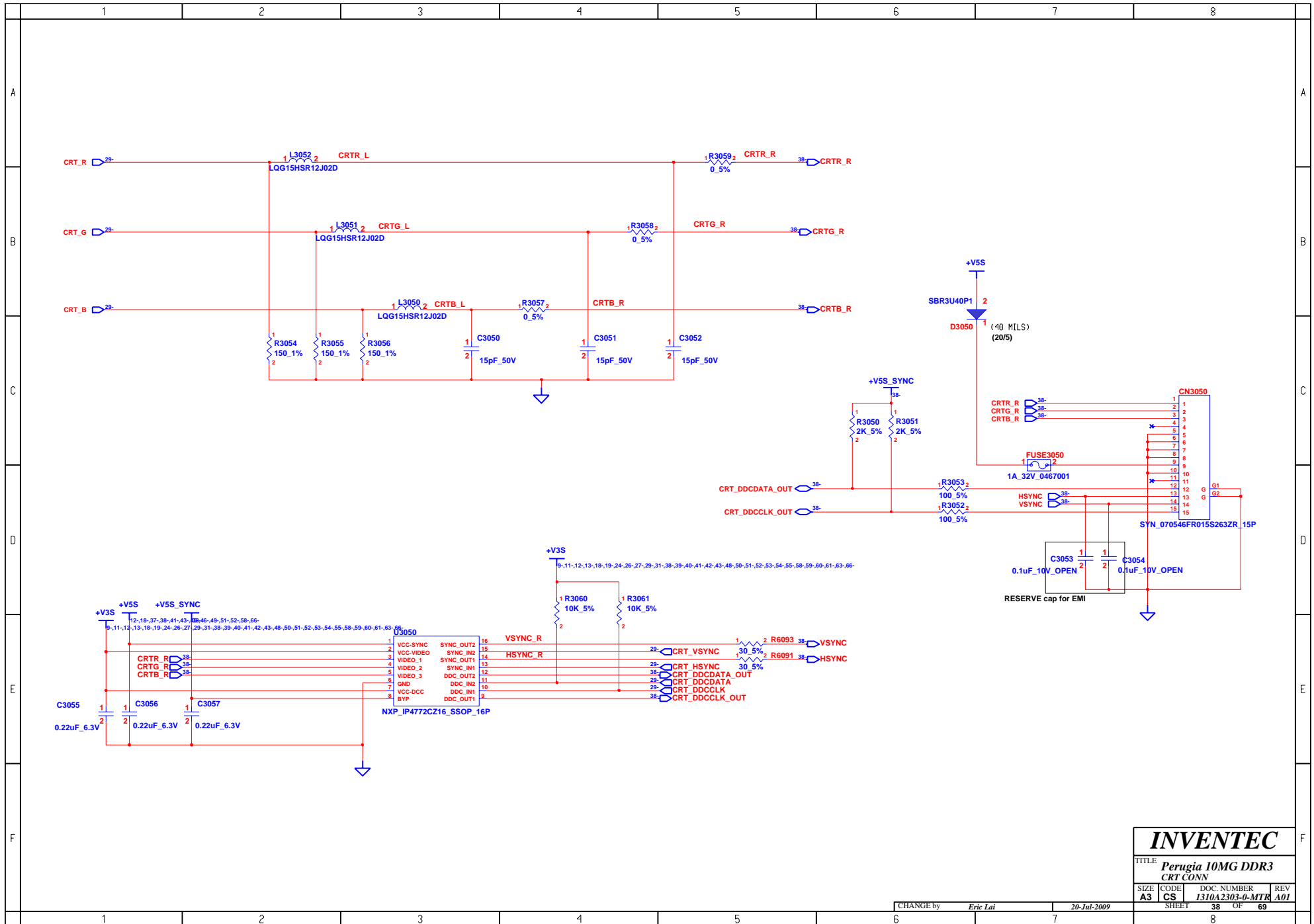
- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

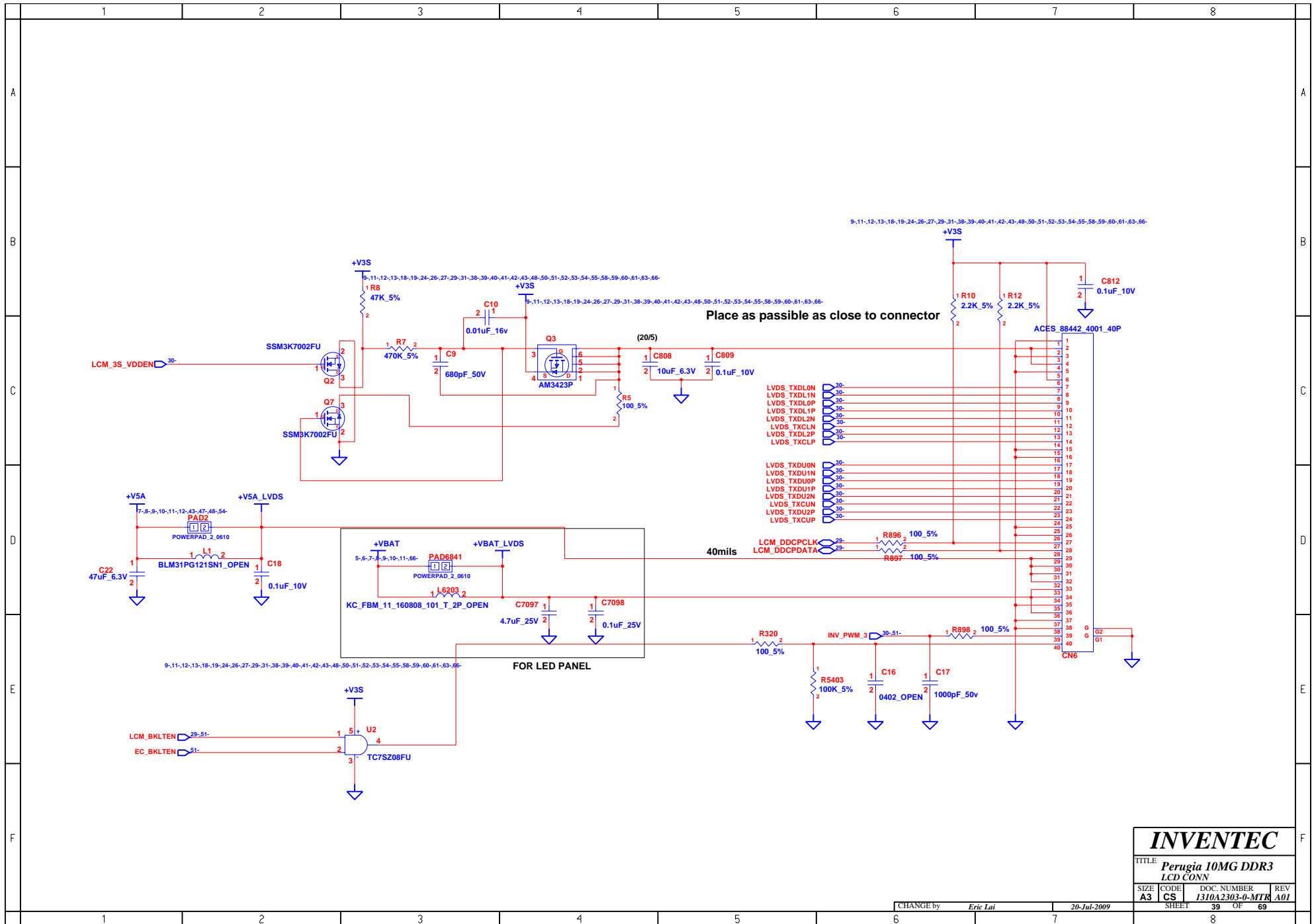
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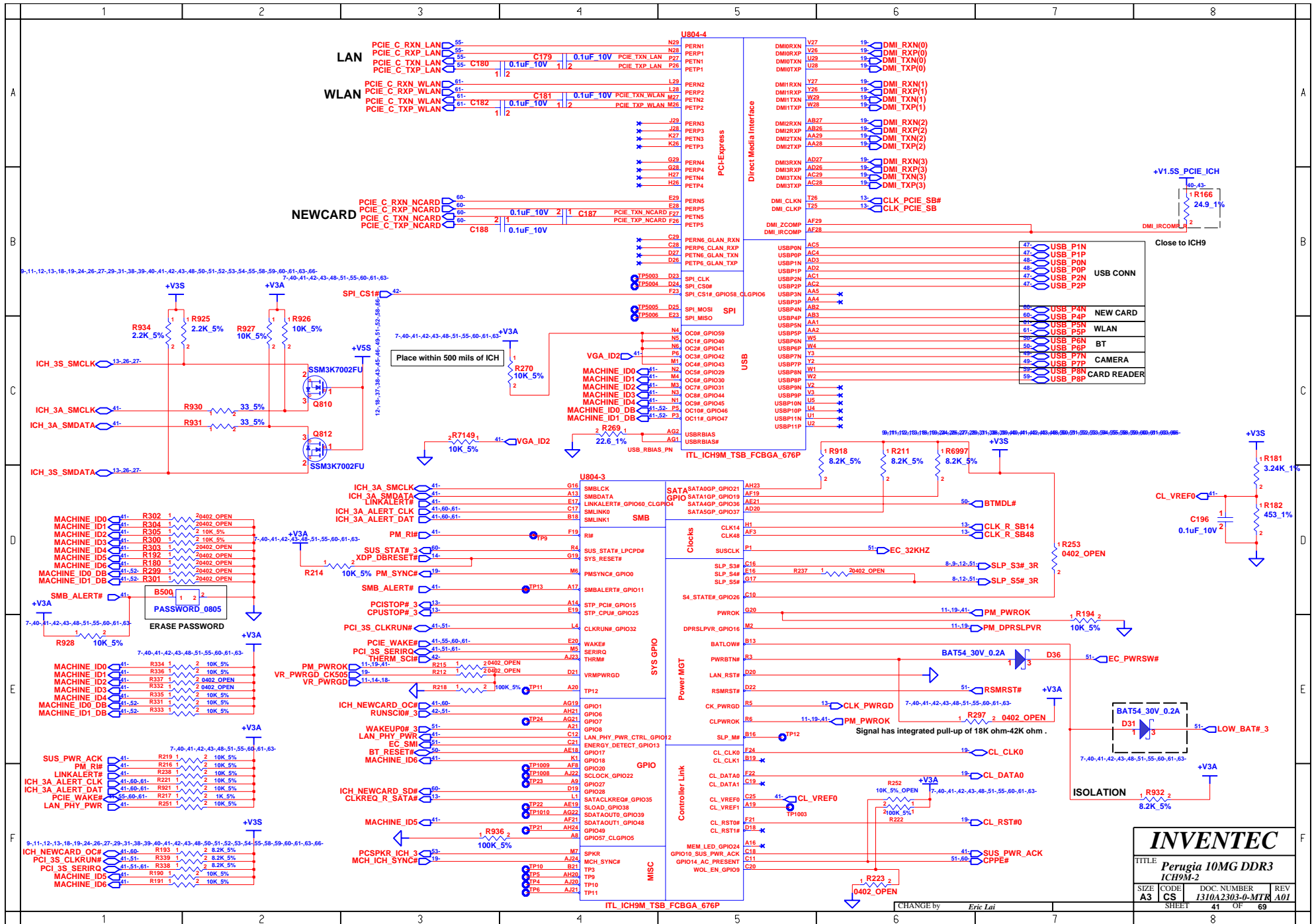
- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 61:** VM R AB(5)
- Pin 66:** VM R AB(6)

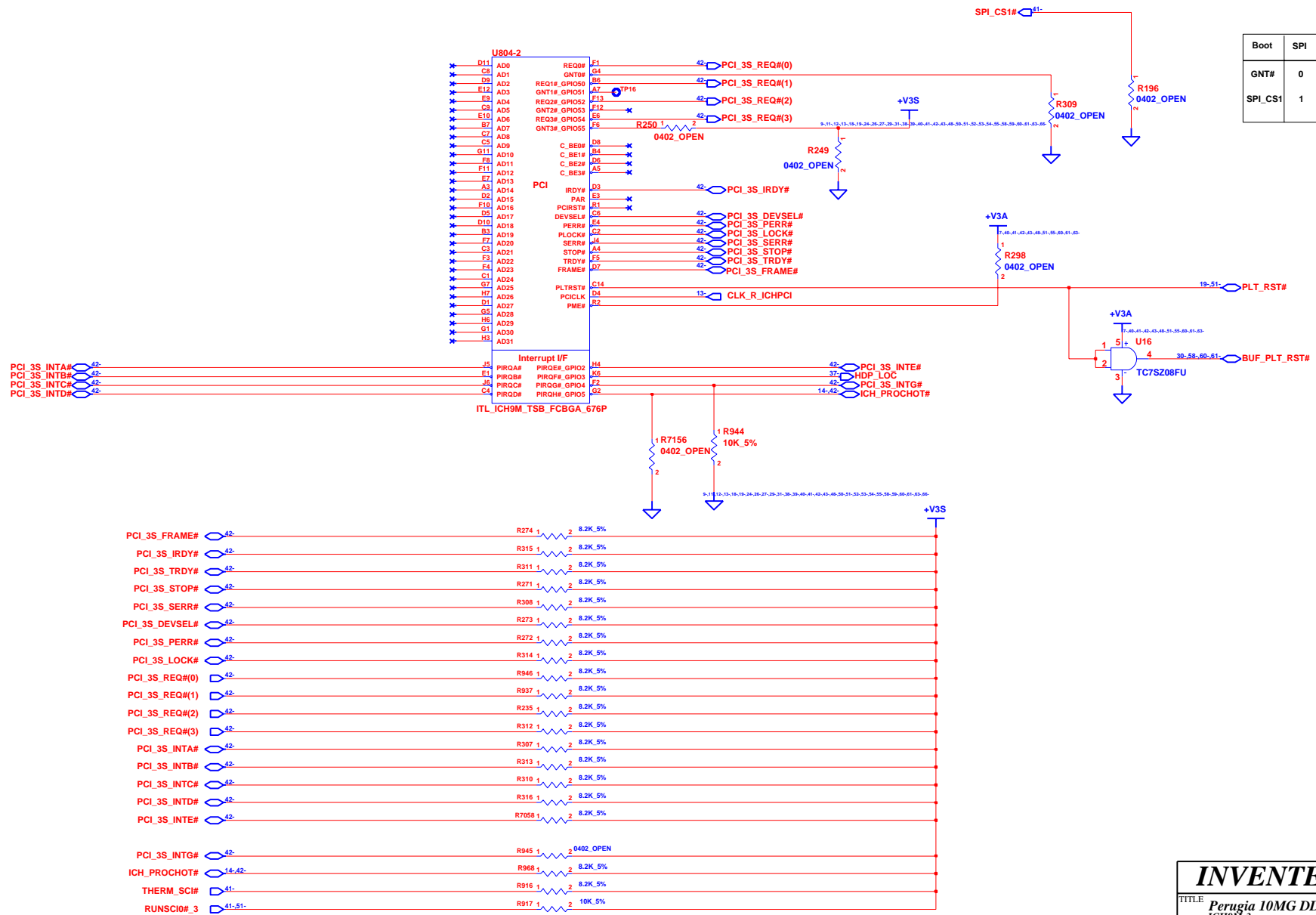
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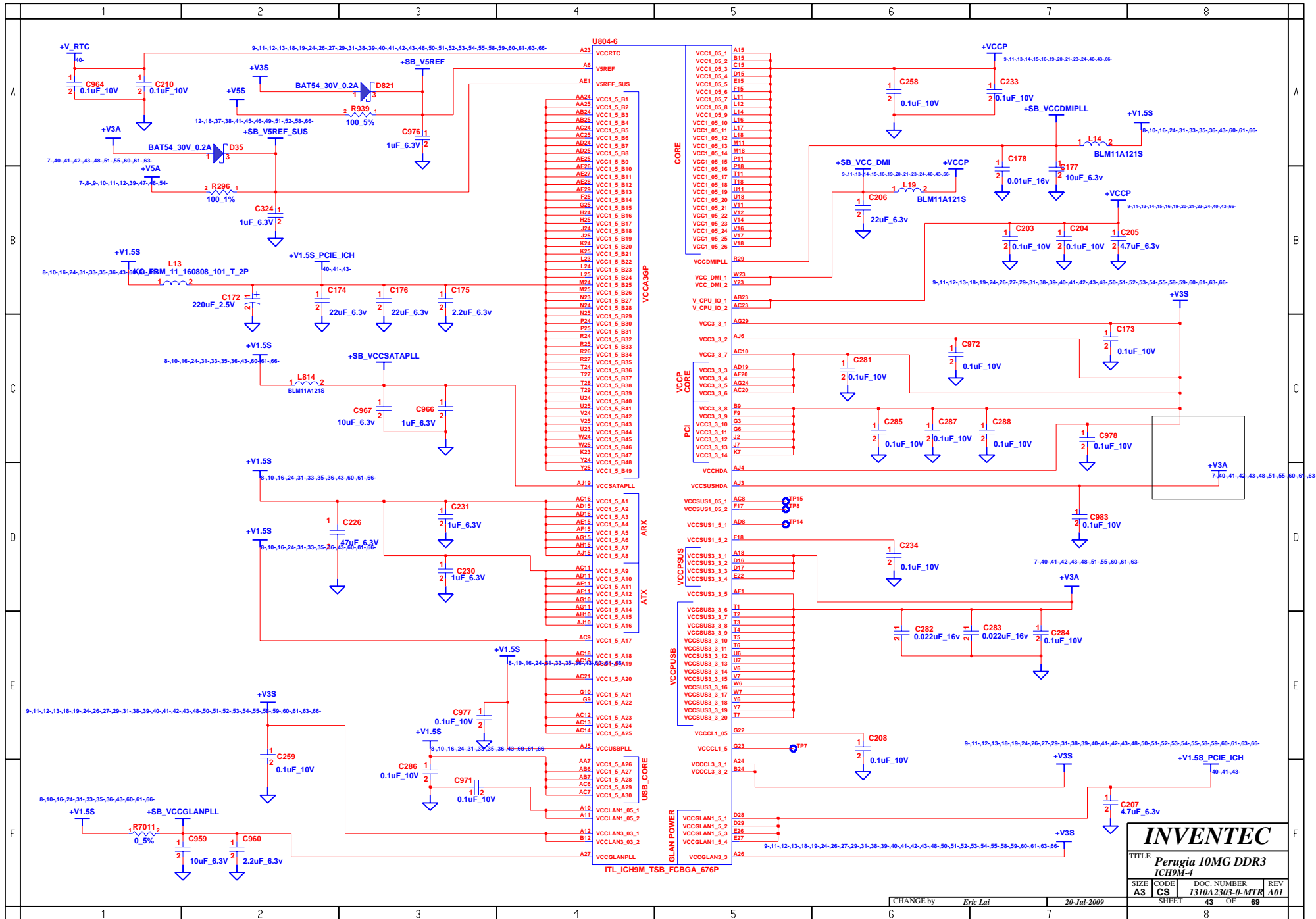
- Pin 33:** VM R AB(0)
- Pin 35:** VM R AB(1)
- Pin 36:** VM R AB(2)
- Pin 43:** VM R AB(3)
- Pin 60:** VM R AB(4)
- Pin 6**





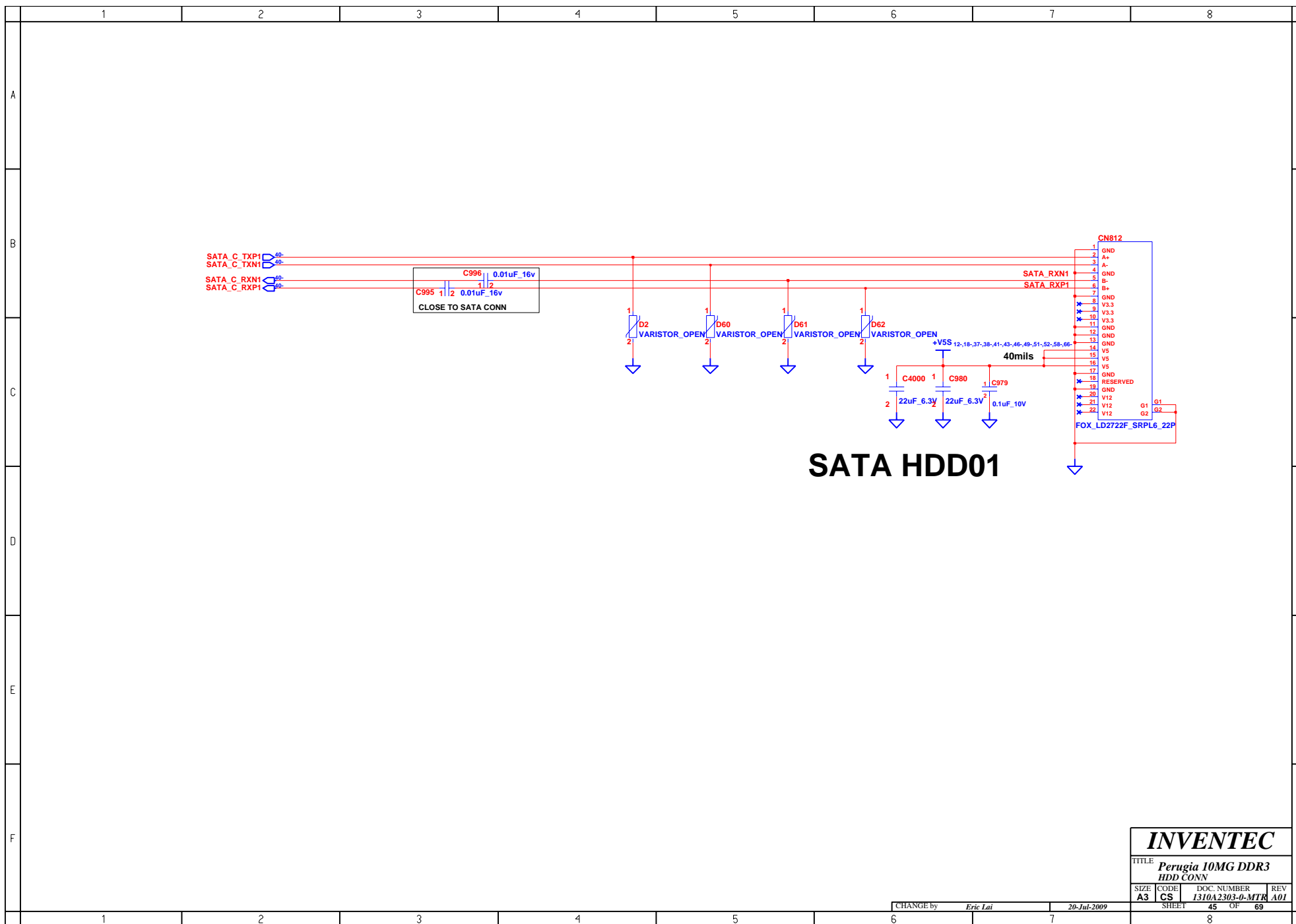




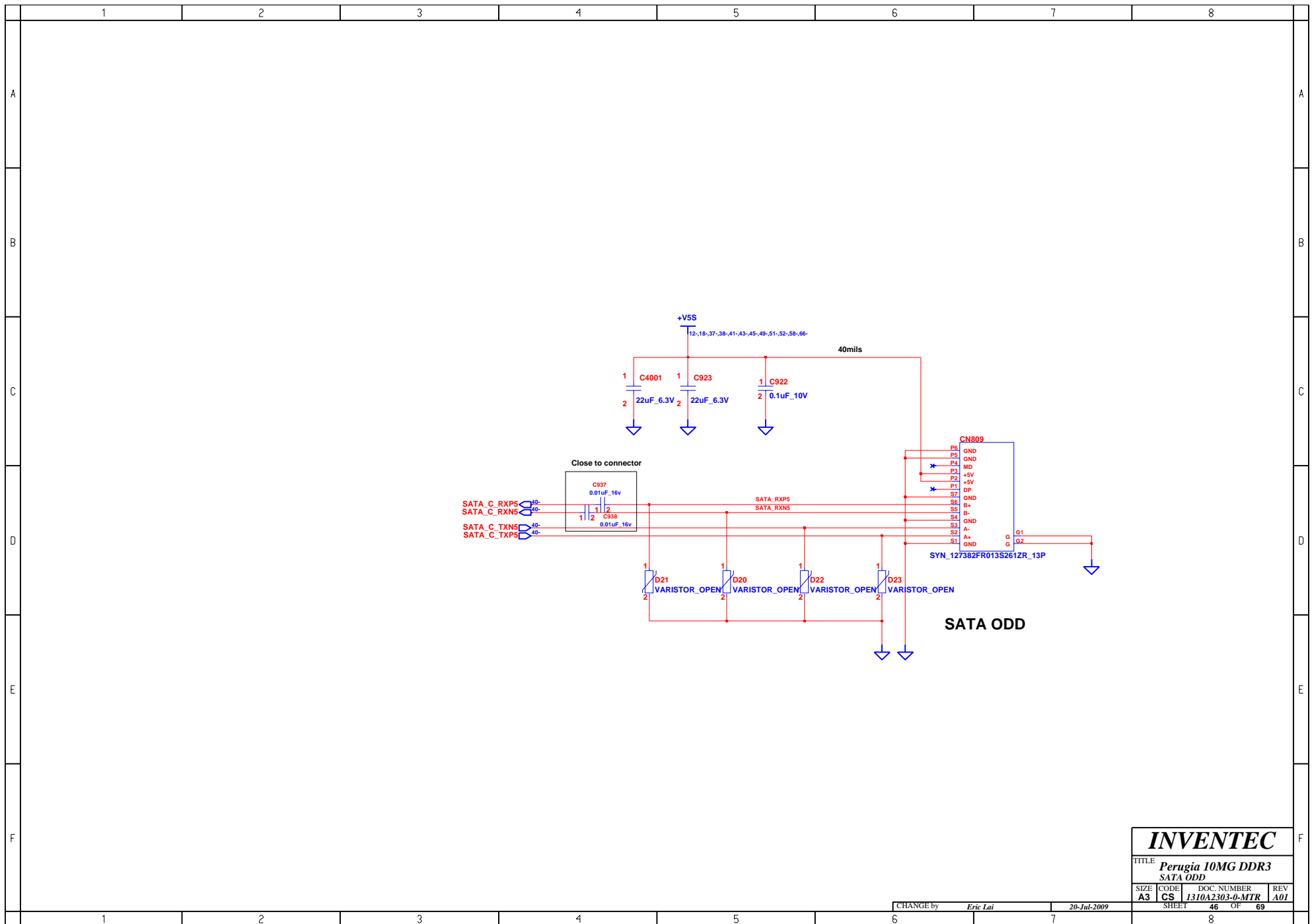


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B								
C								
D								
E								
F								

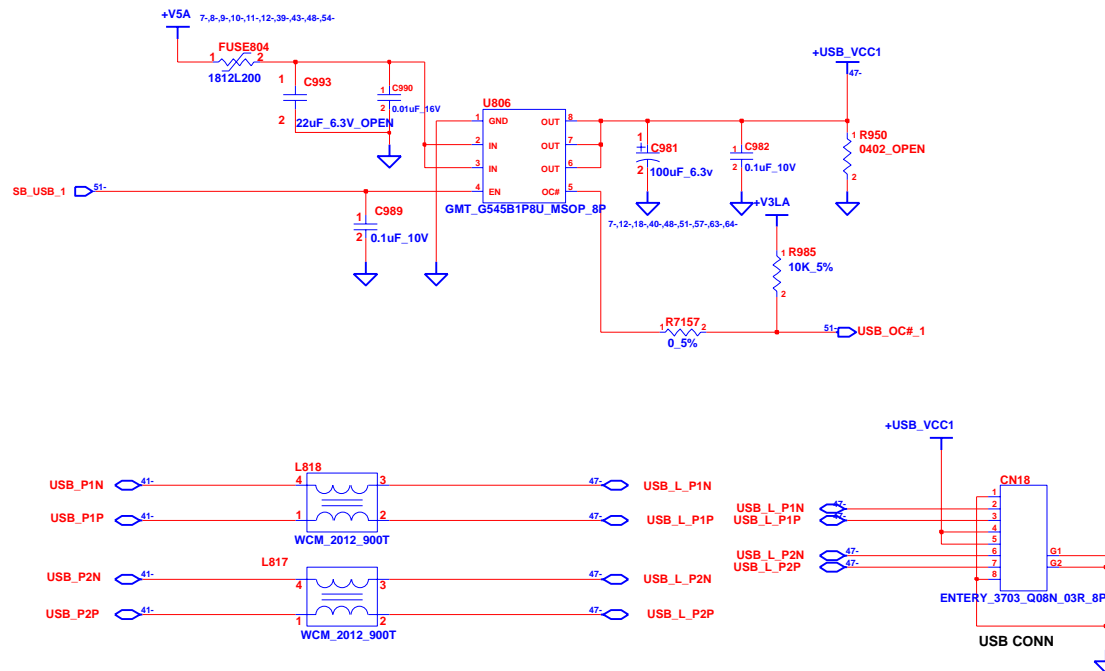
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ICH9M-5			
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CHANGE by Eric Lai		20-Jul-2009	
SHEET 44		OF 69	



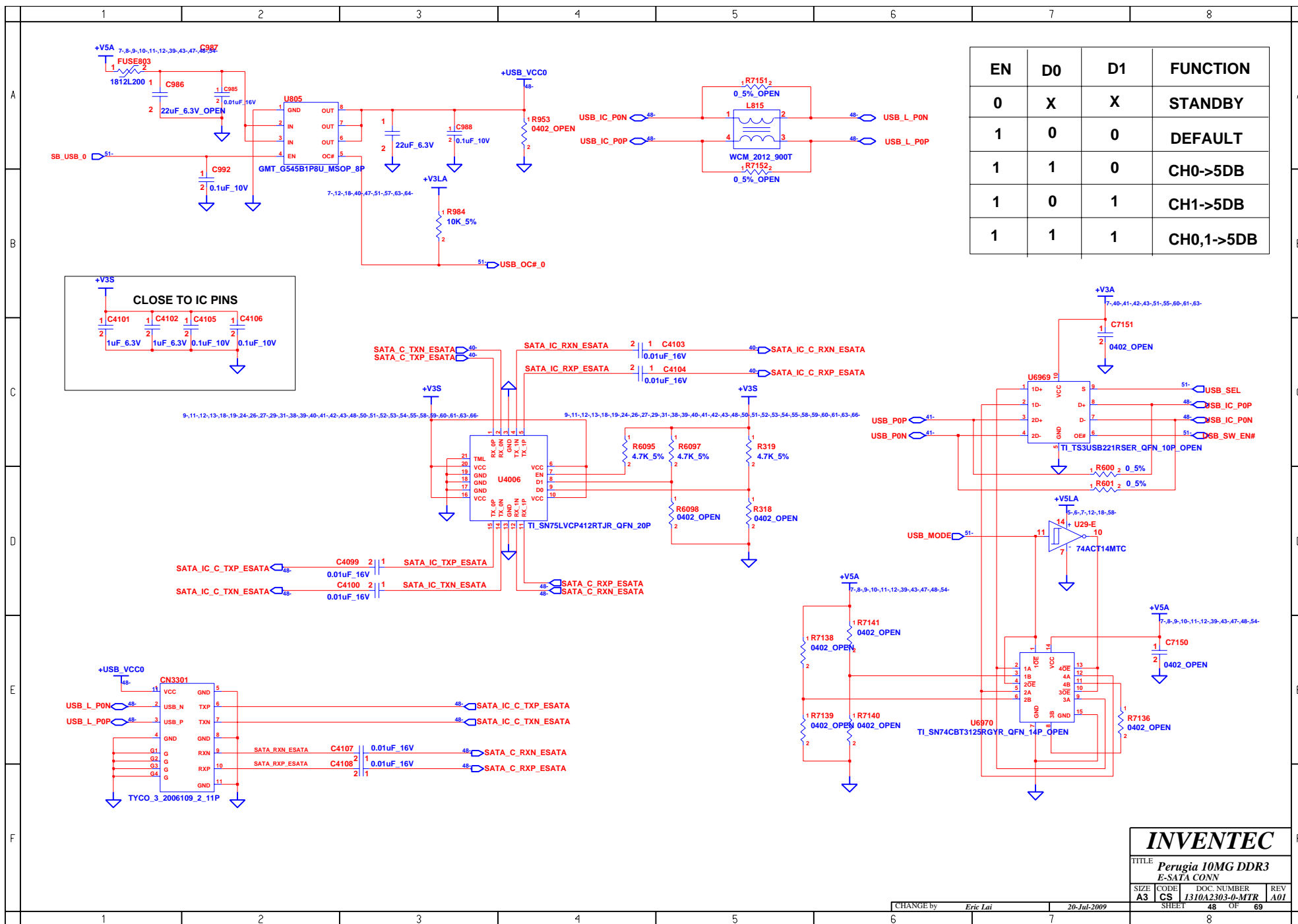
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SIZE A3	CODE CS	DOC. NUMBER I310A2303-0-MTR	REV A01
CHANGE by Eric Lai		20-Jul-2009	
SHEET		45	OF 69

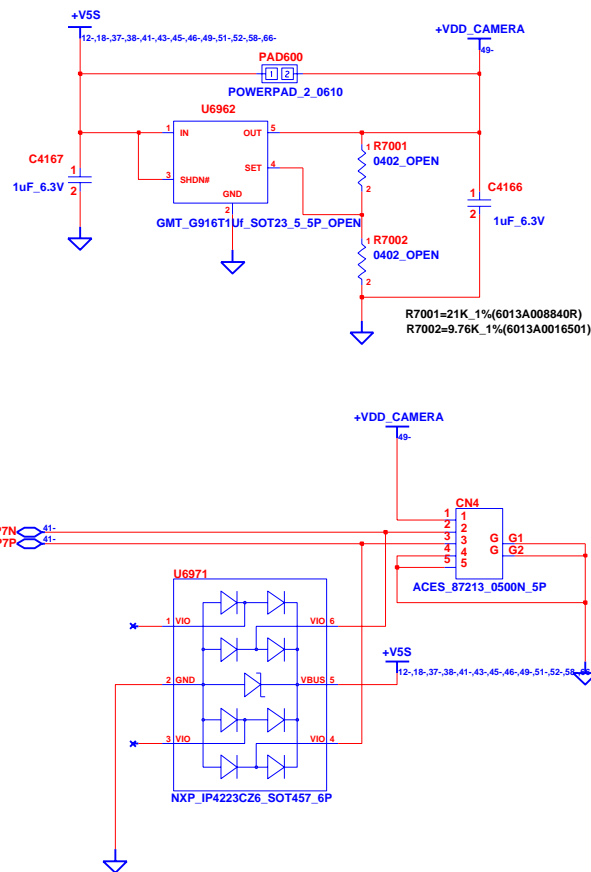


INVENTEC			
TITLE Perugia 10MG DDR3 SATA ODD			
SIZE A3	CODE CS	DOC. NUMBER 1310A2303-0-MTR	REV A01
CHANGE by Eric Lai		20-Jul-2009	
SHEET 46		OF 69	

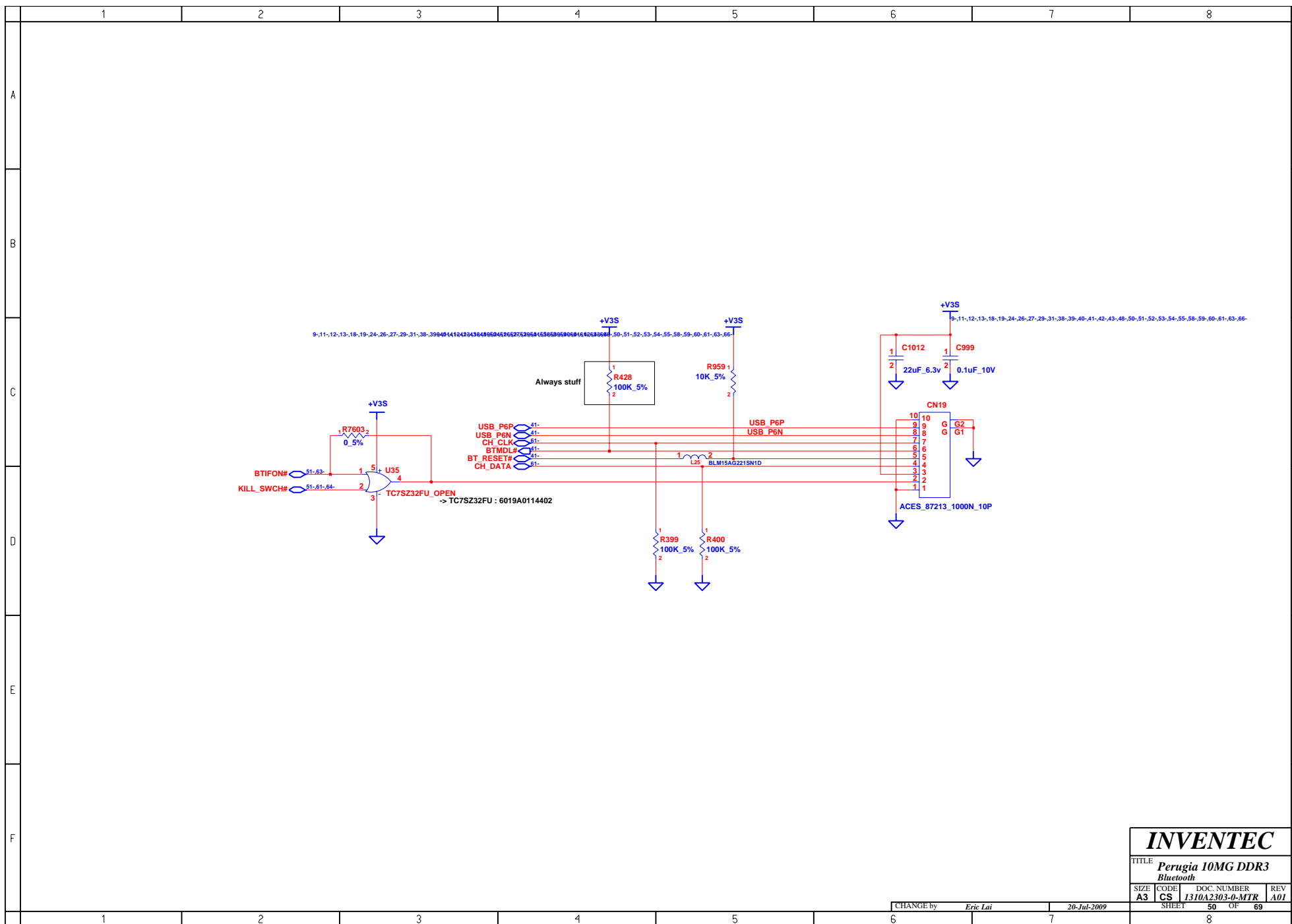


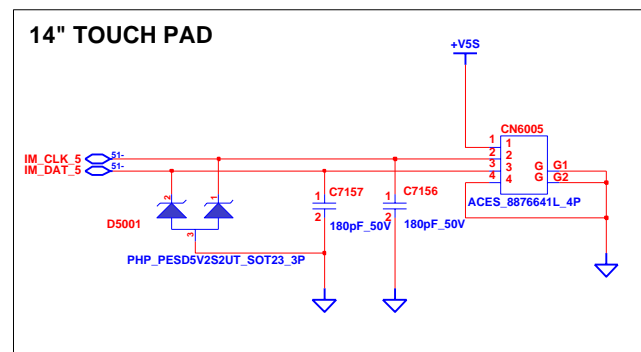
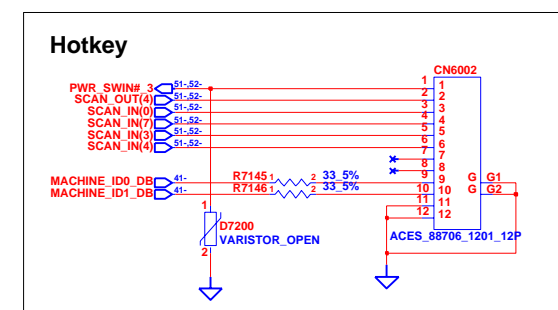
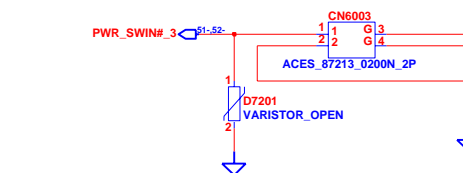
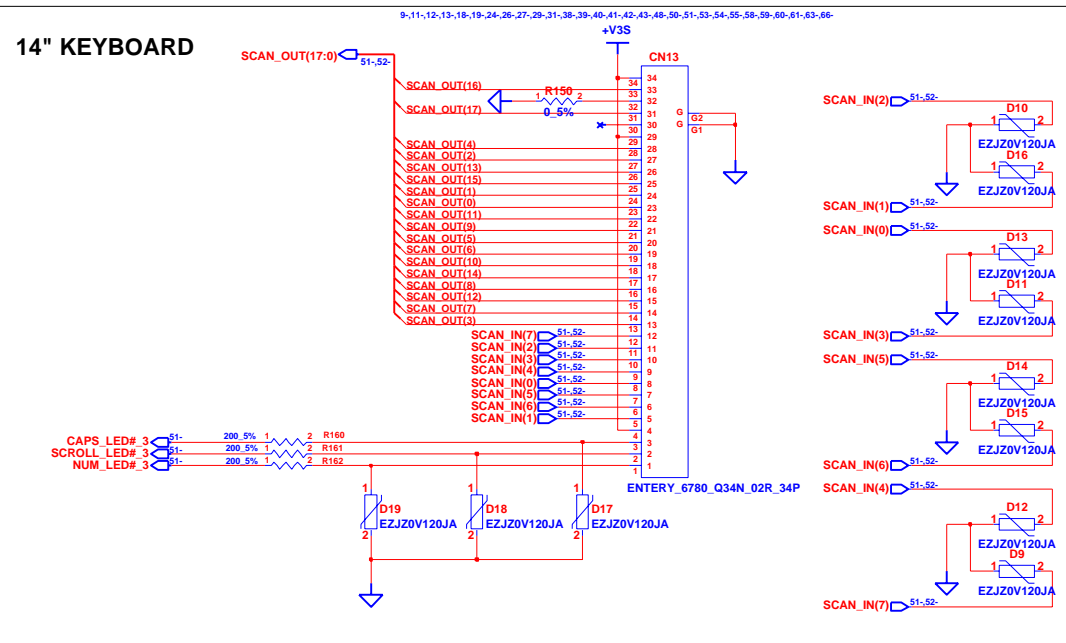
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A3	CS	I310A2303-0-MTR	A01
CHANGE by		Eric Lai	20-Jul-2009
SHEET		47	OF 69





INVENTEC			
TITLE			
Perugia 10MG DDR3 Camera			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A2303-0-MTR	A01
CHANGE by		20-Jul-2009	
SHEET		49	OF 69

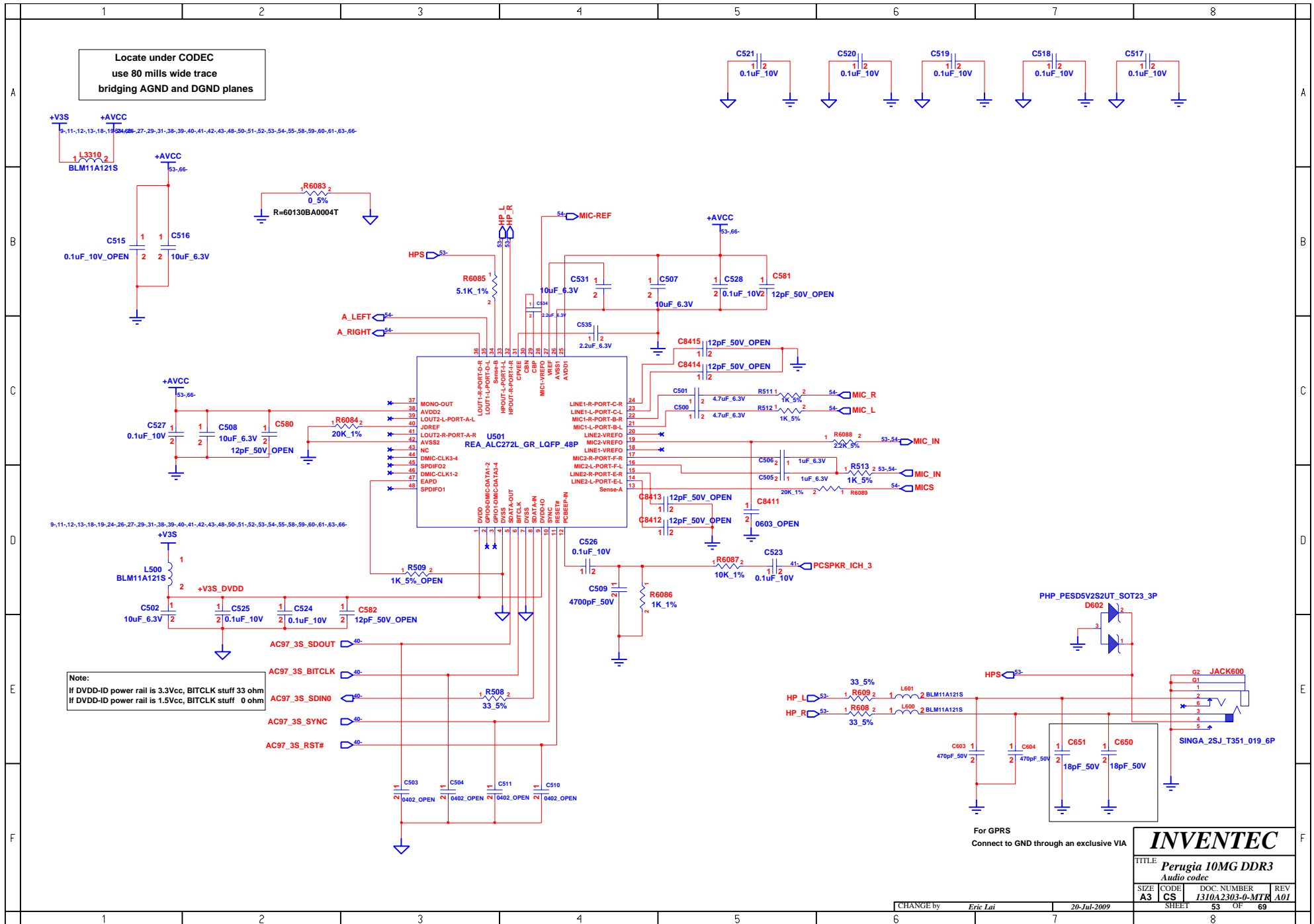


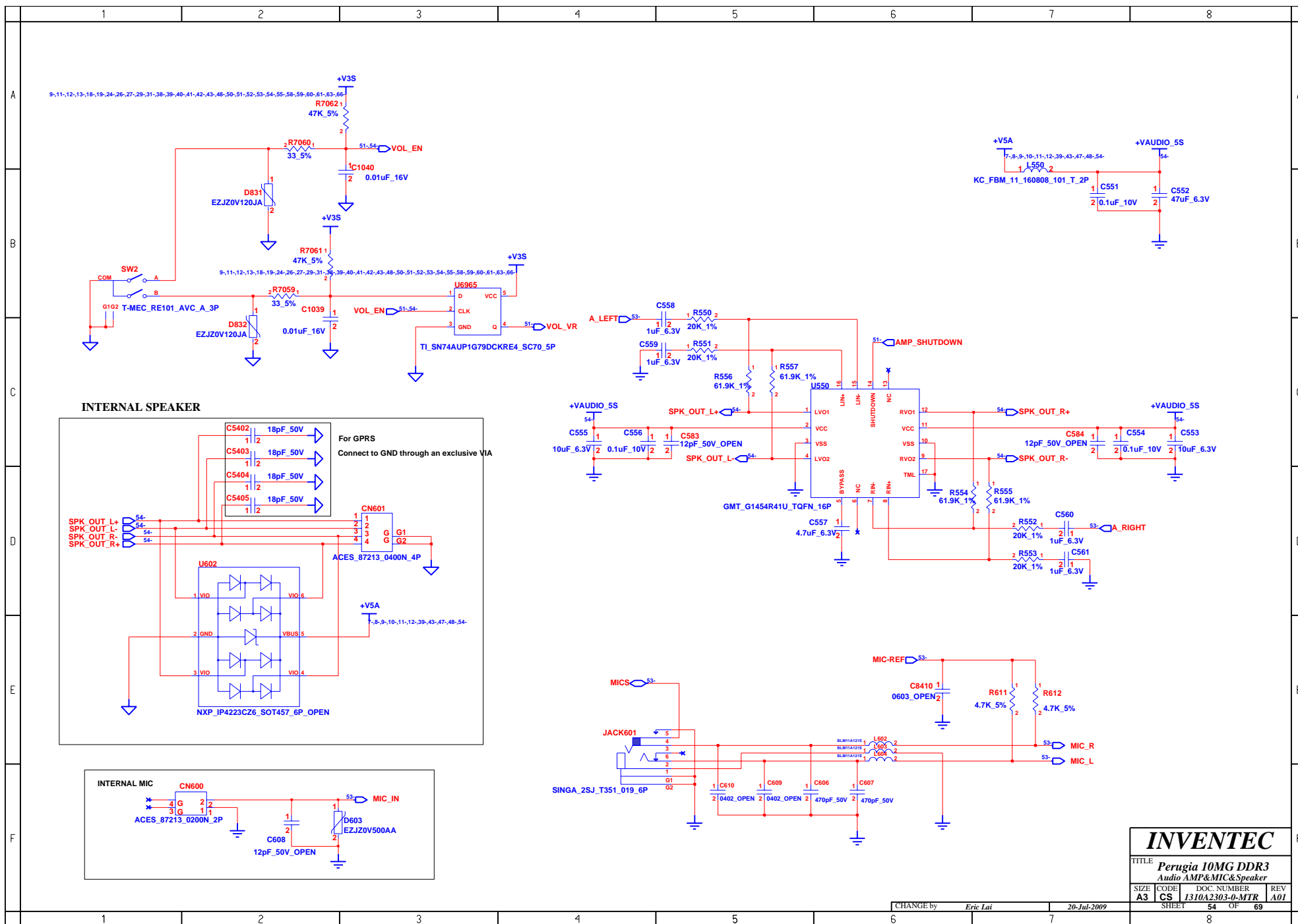


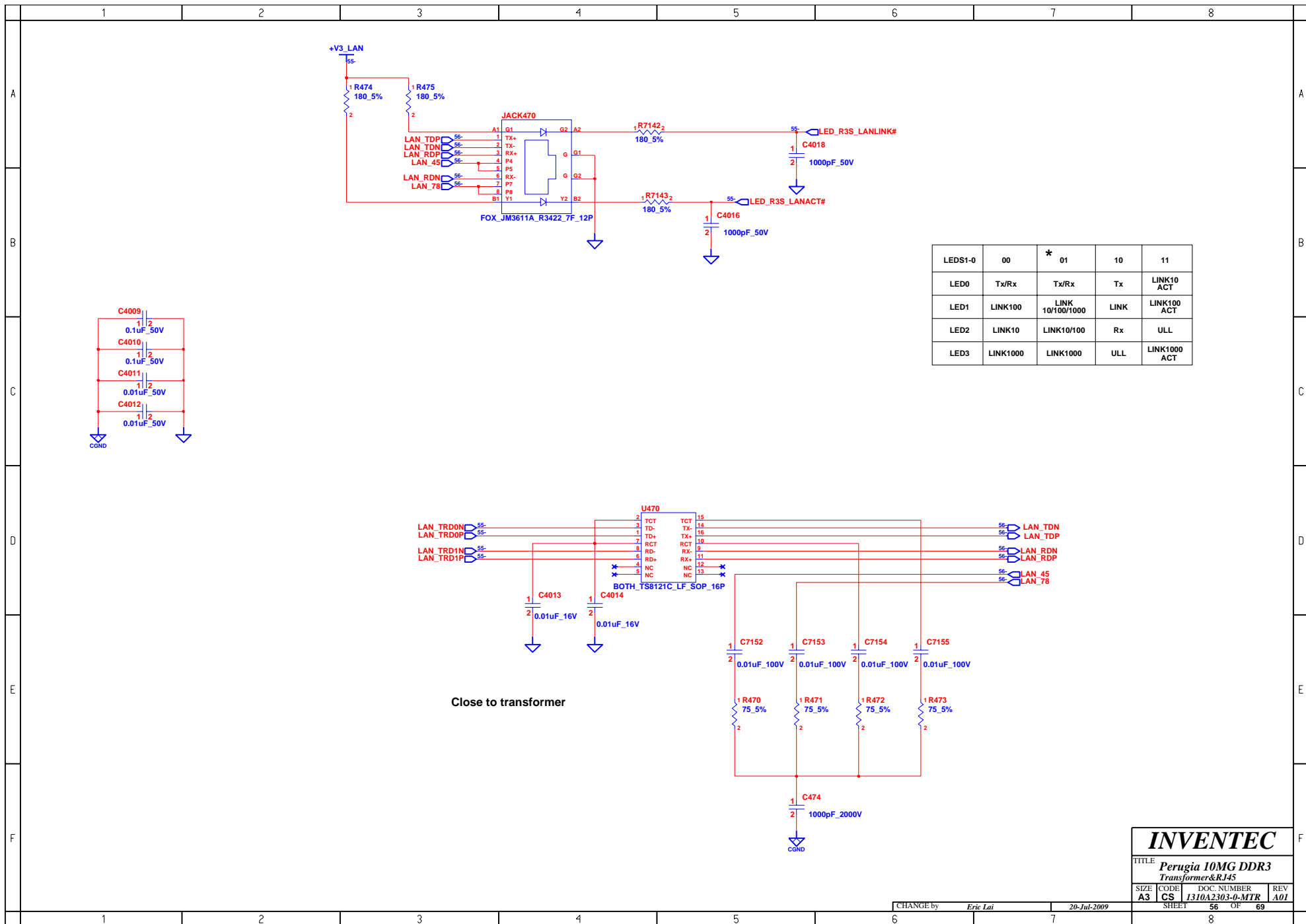
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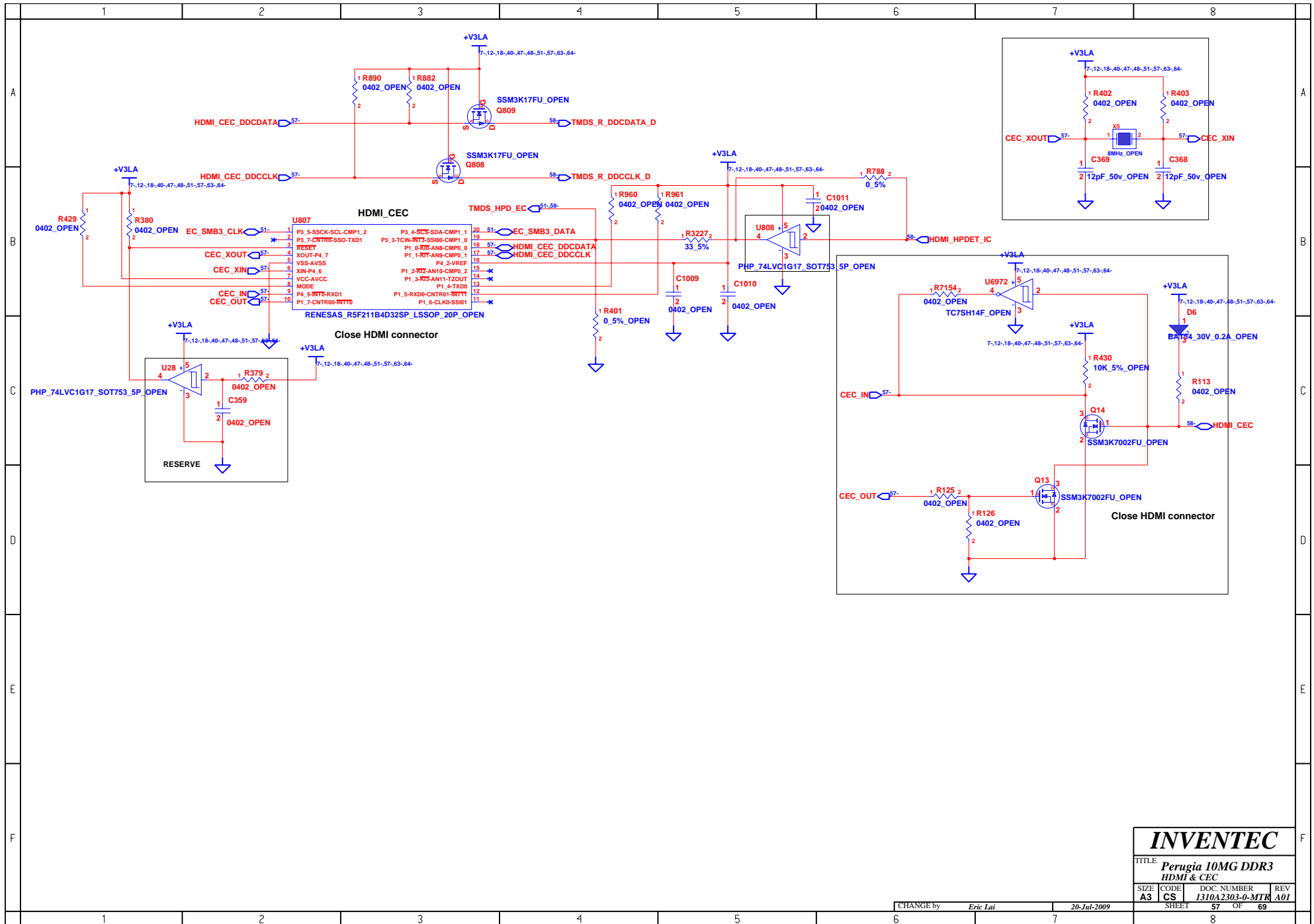
CHANGE by Eric Lai 20-Jul-2009

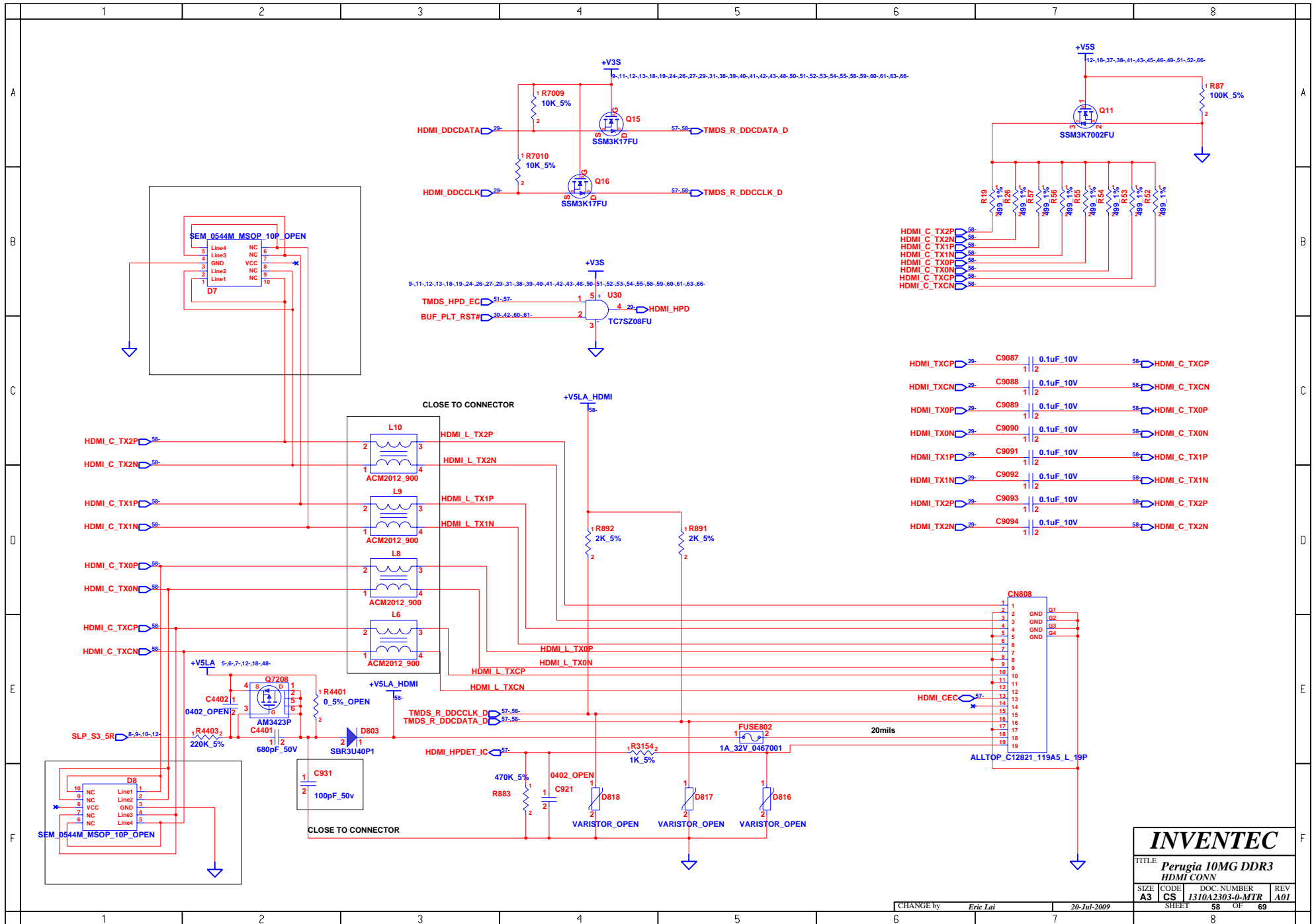
SHEET 52 OF 69

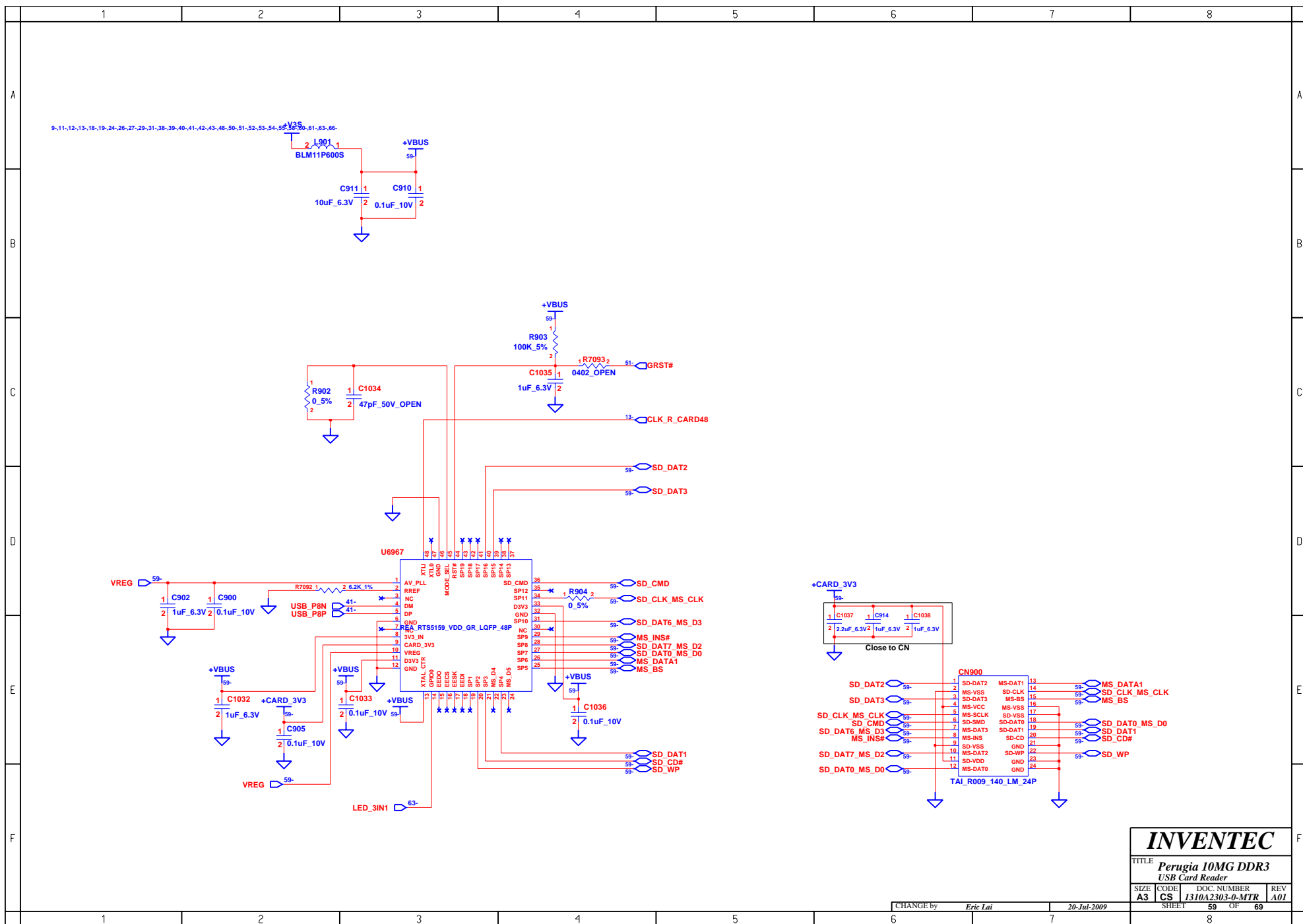


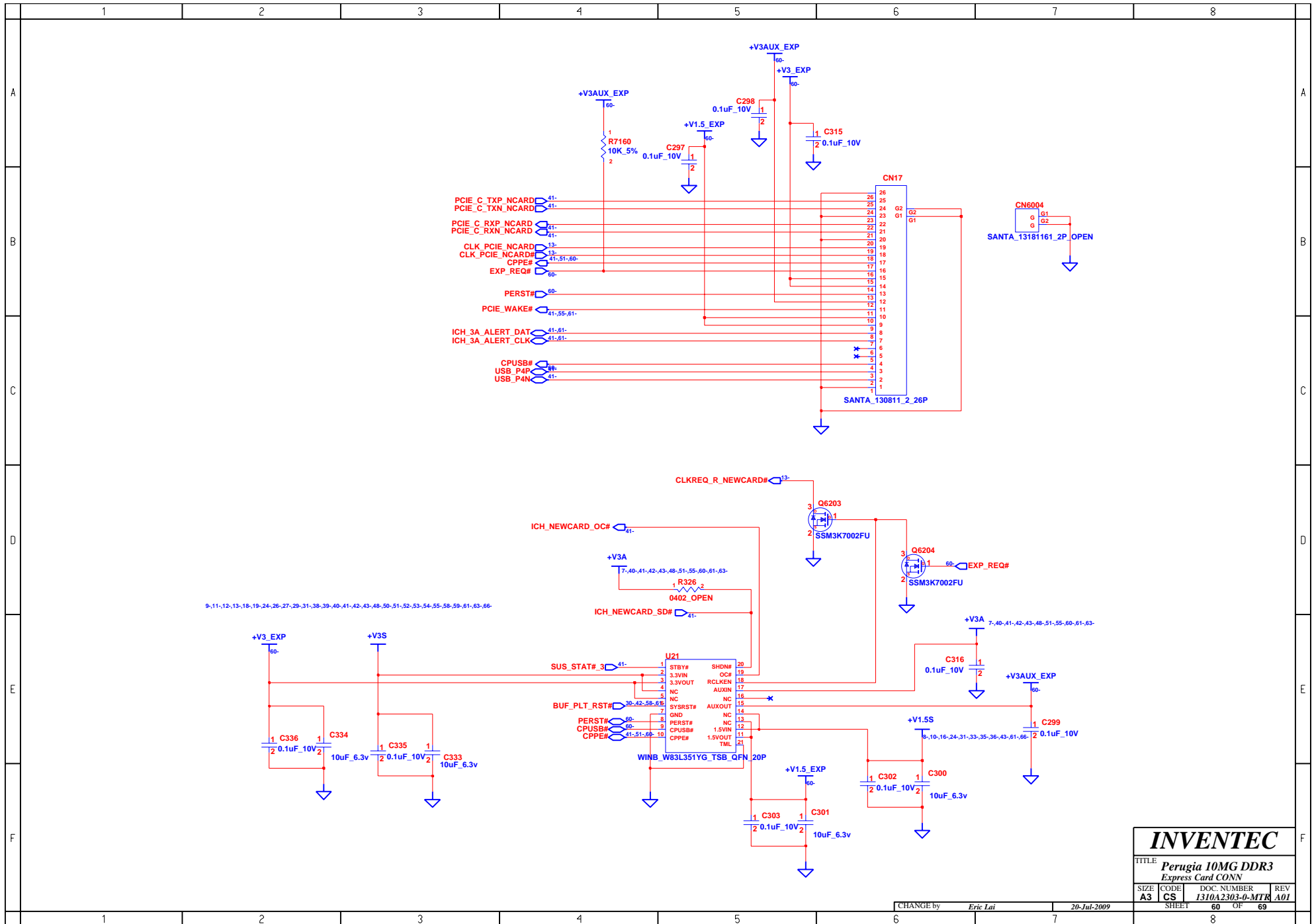




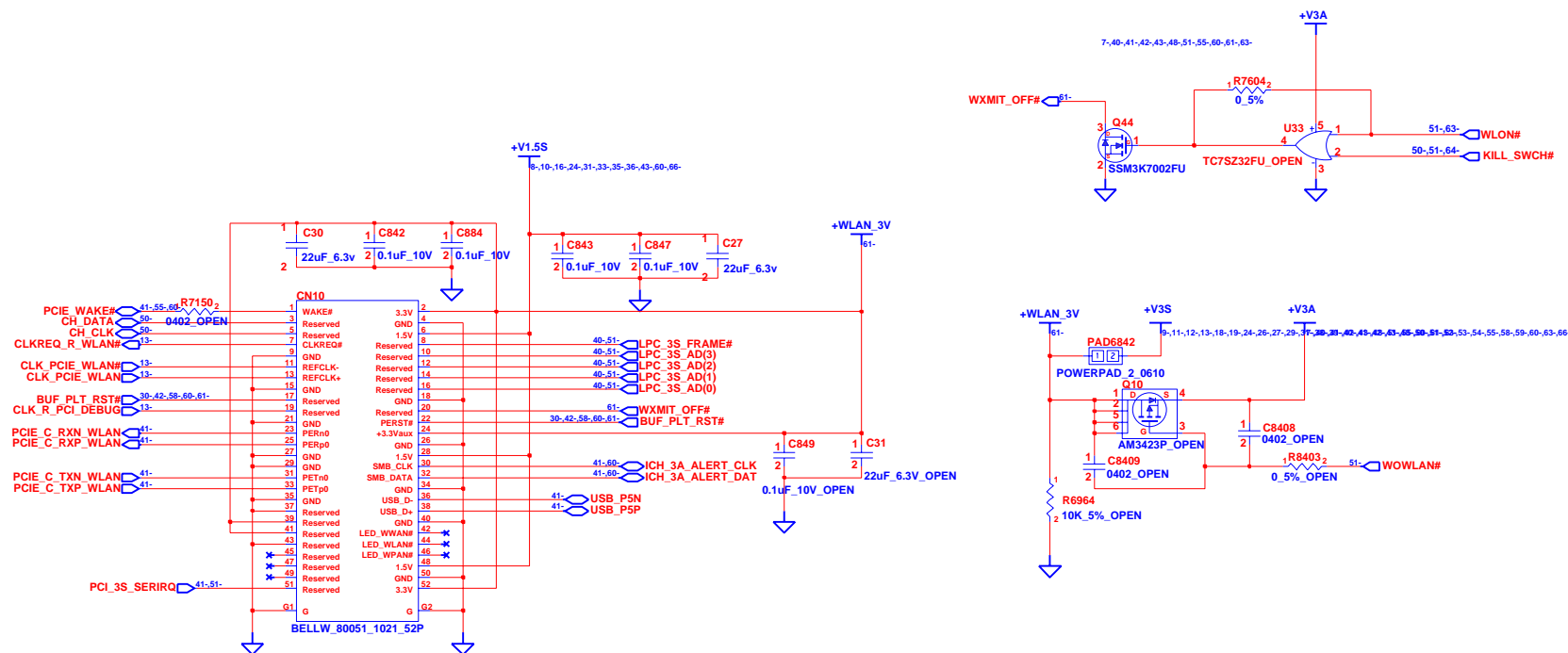








Wireless & Debug card



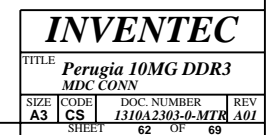
INVENTEC

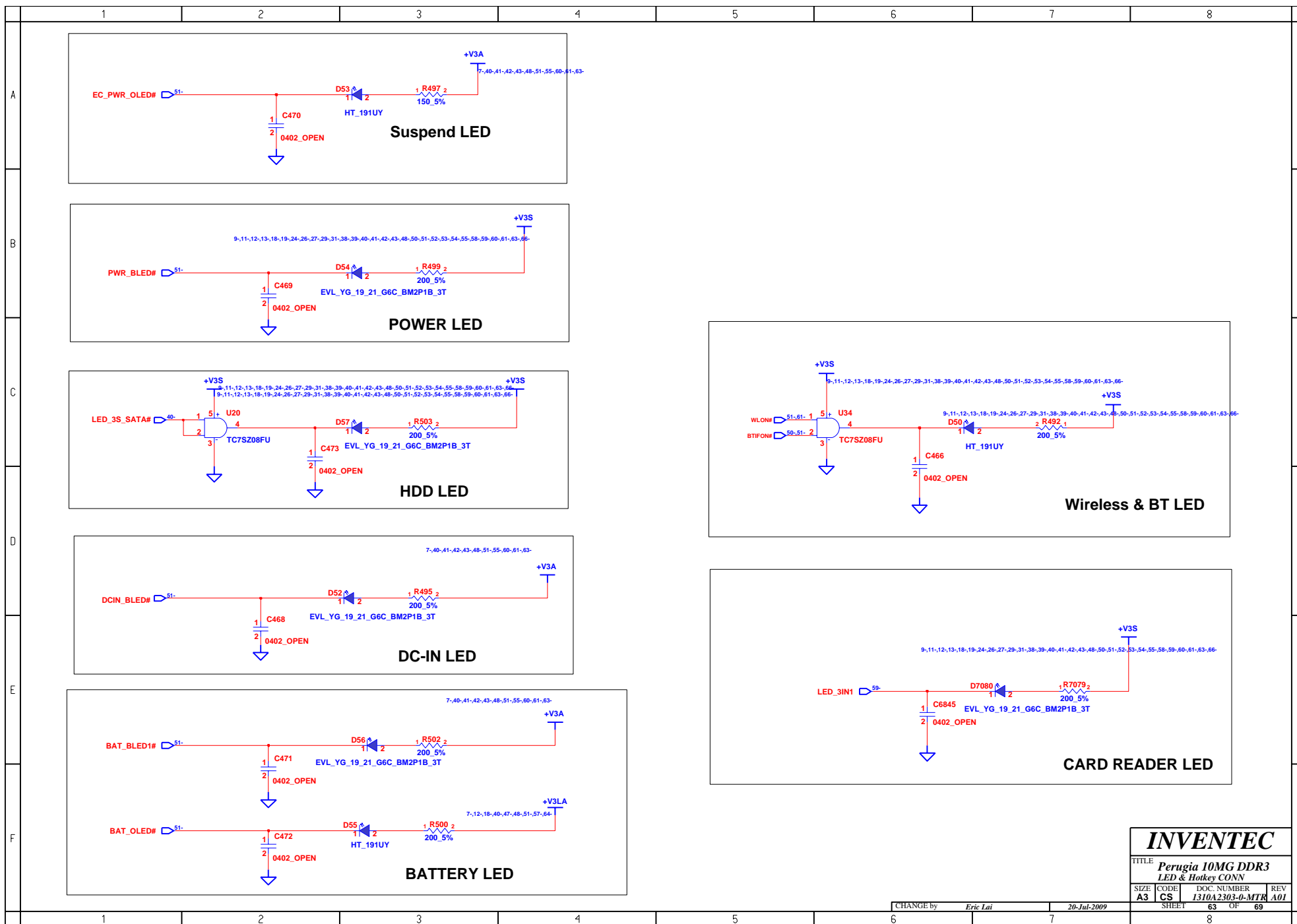
TITLE
Perugia 10MG DDR3
Wireless & debug card

SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A2303-0-MTR	A01

CHANGE by *Eric Lai* 20-Jul-2009

SHEET 61 OF 69

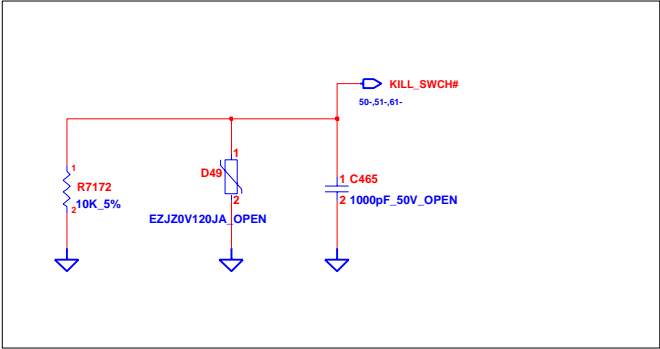




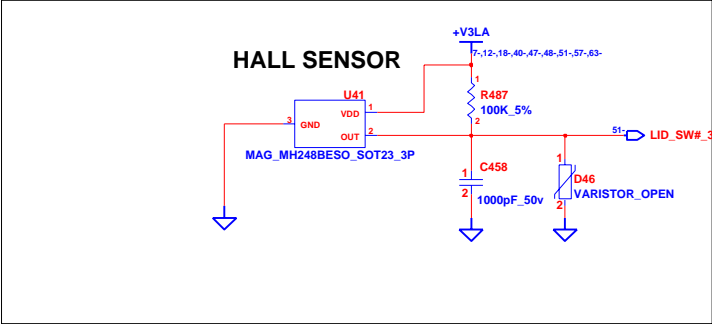
	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F

KILL SWITCH

WLAN ON: KILL_SWCH# -> Low
WLAN OFF: KILL_SWCH# -> High



HALL SENSOR



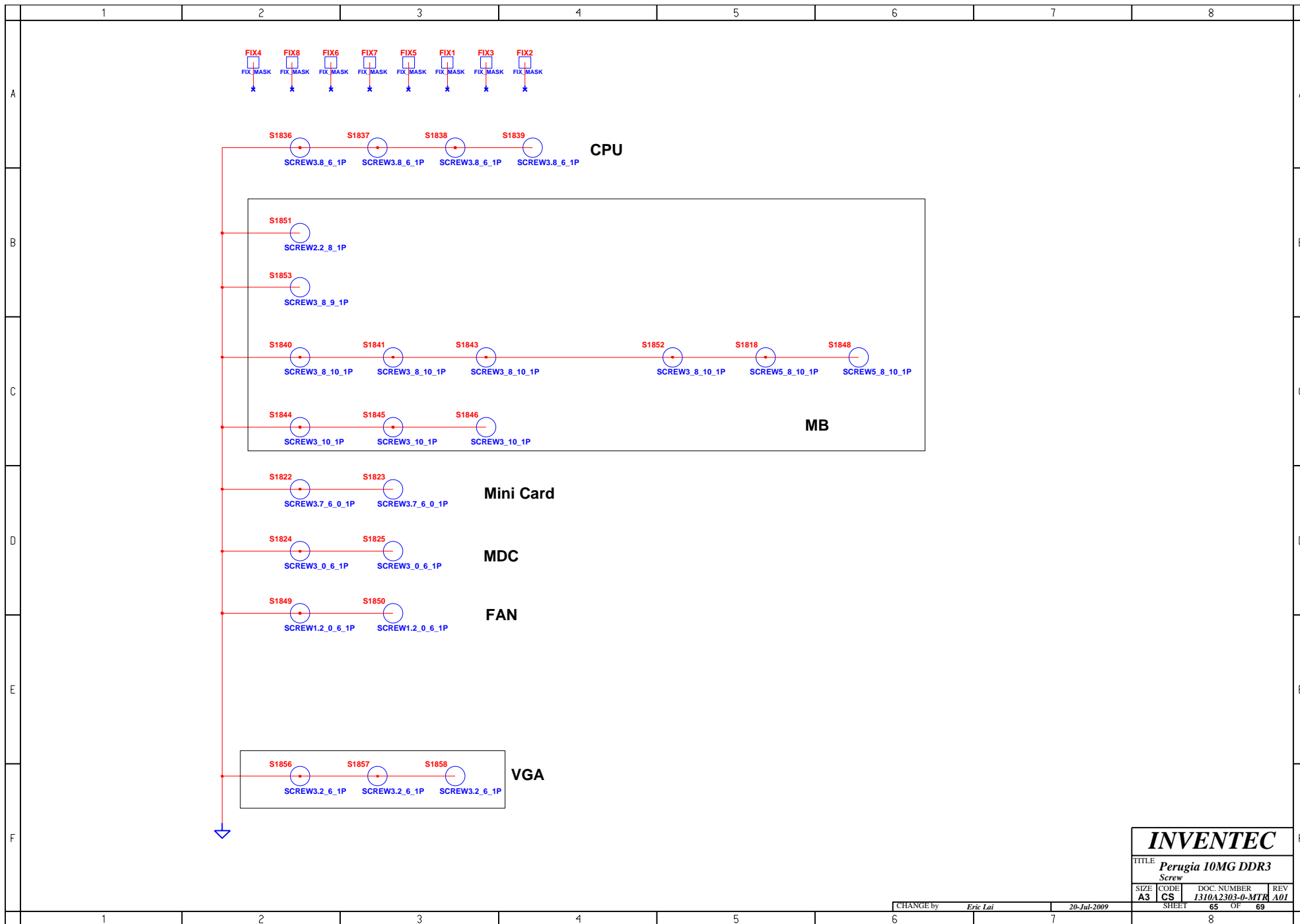
INVENTEC

TITLE
Perugia 10MG DDR3
Kill Swich & Hall Sensor

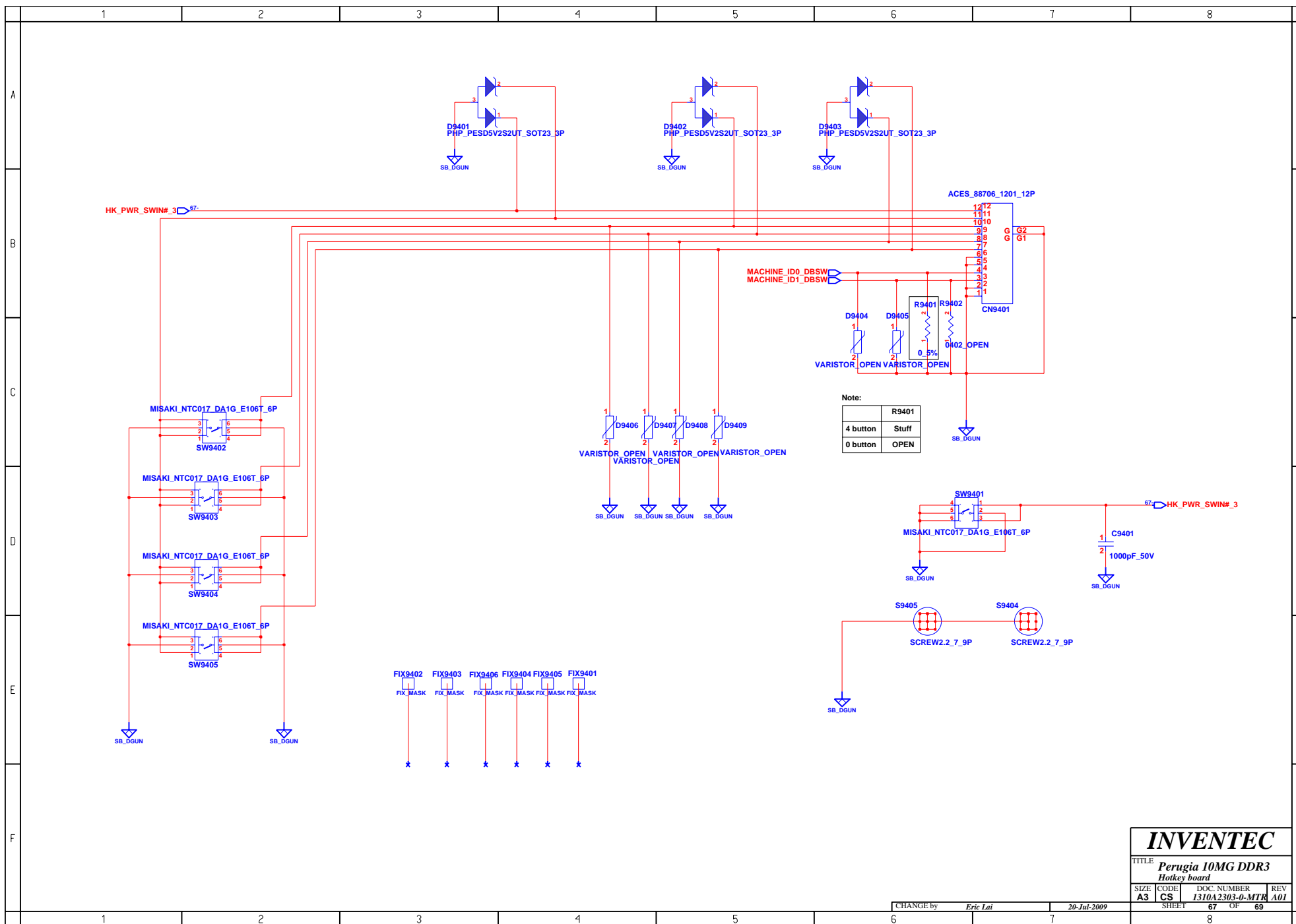
SIZE A3	CODE CS	DOC. NUMBER I310A2303-0-MTR	REV A01
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CHANGE by Eric Lai 20-Jul-2009

SHEET 64 OF 69



INVENTEC			
TITLE			
Perugia 10MG DDR3			
Screw			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A2303-0-MTR	A01
CHANGE by		20-Jul-2009	
Eric Lai			
SHEET		65	OF 69



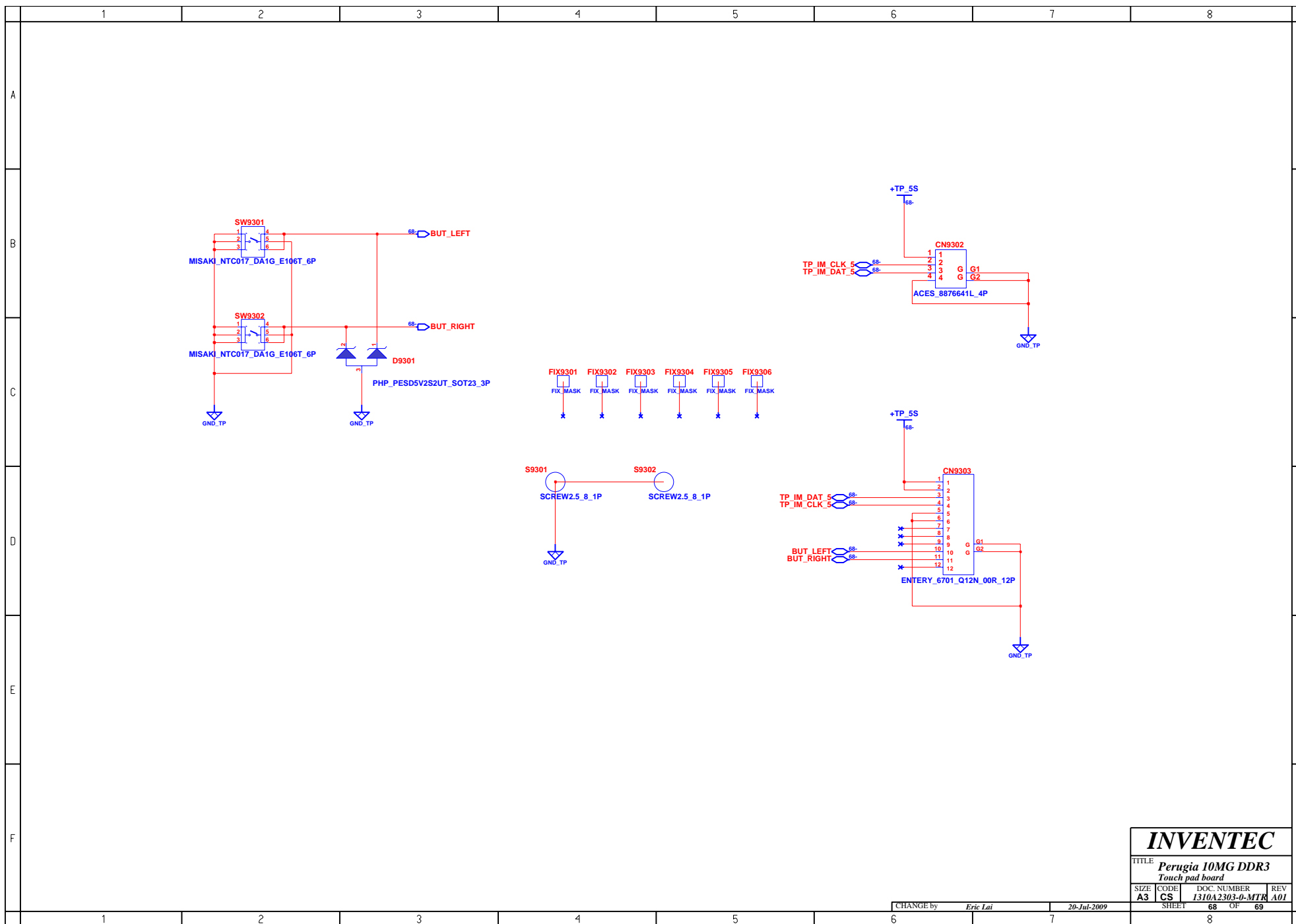
INVENTEC

TITLE
**Perugia 10MG DDR3
Hotkey board**

SIZE CODE DOC. NUMBER REV
A3 CS 1310A2303-0-MTR A01

CHANGE by **Eric Lai** 20-Jul-2009

SHEET 67 OF 69



INVENTEC			
TITLE			
Perugia 10MG DDR3			
Touch pad board			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	I310A2303-0-MTR	A01
CHANGE by		20-Jul-2009	
SHEET		68	OF 69

